

The Role of Quantization Effects on the Operation of 50 nm MOSFET and 250 nm FIBMOS Device

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ABSTRACT

We investigate quantum-mechanical space quantization effects in conventional MOSFET devices and asymmetric device structure fabricated via focused ion beam technique (FIBMOS device). We find that the inclusion of the quantum-mechanical space-quantization effects along the growth direction gives rise to larger average displacement of the carriers from the semiconductor-oxide interface and reduced sheet electron density. This, in turn, leads to threshold voltage shift on the order of 150 to 200 mV, which affects the magnitude of the on-state current and gives rise to transconductance degradation.

Keywords: MOSFETs, asymmetric device structures, space-quantization effect, threshold voltage degradation, on-state current degradation

1 INTRODUCTION

The end of the CMOS scaling is foreseeable, although the specific combination of factors that will end scaling is not known. As industry moves through the two to three year technology generation cycles, the complexity of the processes is increasing and the demands on fabrication equipment performance are more strenuous. For example, in order to fabricate a 25 nm device, lithography tools are needed that operate beyond optical lithography limits. The performance of the scaled device in the 25 nm regime is itself problematical. The gate oxide has to be aggressively scaled to enhance device performance. However, as the thickness of the gate approaches 1 nm through scaling, tunneling through the gate oxide creates unacceptably large off-state currents, dramatically increasing quiescent power consumption, and rendering the device impractical for analog applications due to unacceptable noise level. Source to drain tunneling also contributes to the off-state current.

Another issue that will pose serious problems on the operation of future ultra-small devices is related to the discrete nature of impurity atoms. The distribution of dopants is traditionally treated as continuum in semiconductor physics that implies (a) the number of impurity atoms is small as compared to the total number of atoms in the semiconductor matrix; (b) the impurity atoms distribution is statistically uniform, while the position of an individual atom in the lattice is not defined, e.g. is random. The assumption of statistical uniformity requires large number of atoms, which is not the case in, let's say, 25 nm MOSFET device in which one has less than one hundred dopant atoms in the junction

region. In these future ultra-small devices, the number and location of each dopant atom will play an important role in determining the device behavior. The challenge of precisely placing small numbers of dopants may represent a brick wall and could end conventional MOSFET scaling.

For the proper description of all of these issues, it is necessary to have simulation tools that go beyond the drift-diffusion and hydrodynamic models traditionally used in the Industry. In addition, for more exact treatment of discrete impurity effects, it is mandatory to have three-dimensional (3D) rather than two-dimensional (2D) simulation tools. Moreover, instead of considering a single device, one has to analyze an ensemble of devices with different number and different distribution of the impurity atoms. A solution to this dilemma, while still limiting itself to the realm of semiclassical transport approach, is to use 2D and 3D particle-based simulators based on the numerical solution of the Boltzmann transport equation via the Monte Carlo technique. The only drawback to these methods is the CPU time needed for solving either the 2D or the 3D Poisson equation used for calculating the electric field that drives the carriers during the free-flight sequence of the Monte Carlo transport kernel.

However, even though sophisticated Monte Carlo particle-based solvers have been developed by various research groups (based on analytic or a full-band structure), they still lack an important element. Namely the proper incorporation of the quantum-mechanical space-quantization effects, that arise in state-of-the-art devices due to the very high substrate doping used to prevent the punchthrough effect, is still missing. One consequence of the space-quantization effect is higher average displacement of the carriers from the interface proper, which leads to effective oxide thickness increase and total gate capacitance degradation. Additional degradation of the total gate capacitance arises from the poly-depletion effects that lead to additional capacitance component in series with the oxide and the inversion layer capacitance. The total gate-capacitance degradation due to these two effects is clearly seen in Figure 1, where we show the total gate capacitance for different technology generations (as a function of the oxide thickness). We use Fermi-Dirac (F-D) and Maxwell-Boltzmann (M-B) statistics for the case of classical charge description and F-D statistics for the case of quantum-mechanical charge description. From the results shown in Figure 1, it follows that the quantum-mechanical charge description leads to approximately 20% degradation of the total gate capacitance when compared to the classical charge description model for the end of the roadmap devices with oxide thickness between 1 and 1.5 nm. Further capacitance degradation, up to 40% for

the smallest oxide thickness, is due to the additional poly-depletion effect. The total gate capacitance degradation, on the other hand, when combined with the quantum-mechanical band-gap widening effect due to the reduced density of states, gives rise to a reduction of the sheet electron density. This, in turn, increases the threshold voltage and, at the same time, degrades the device transconductance. Hence, to properly describe the operation of future ultra-small devices, it becomes mandatory to incorporate quantum-mechanical and poly-depletion effects into the existing device simulators.

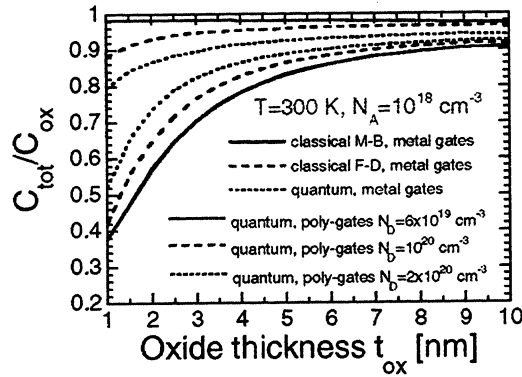


Figure 1: Total gate capacitance as a function of the oxide thickness.

One way of incorporating quantum-mechanical space-quantization effects is to use 1D or 2D Schrödinger equation solvers coupled with existing particle-based simulator. This is not practical, however, because the repeated solution of the Schrödinger equation adds in to the required CPU time. There have been several interesting proposals in the past that avoid this problem. All of them are based on the idea of quantum potentials that derive from the hydrodynamic formulation of quantum mechanics first introduced by de Broglie and Madelung [1,2,3] and later developed by Bohm [4,5]. In this picture, the wave function is written in complex form in terms of its amplitude and phase, and, when substituted back into the Schrödinger equation leads to coupled equations of motion for the density and phase, of the form

$$\frac{\partial \rho(\mathbf{r}, t)}{\partial t} + \nabla \cdot \left(\rho \frac{1}{m} \nabla S \right) = 0, \quad (1)$$

$$-\frac{\partial S(\mathbf{r}, t)}{\partial t} = \frac{1}{2m} (\nabla S)^2 + V(\mathbf{r}, t) + Q(\rho, \mathbf{r}, t), \quad (2)$$

where the probability density is $\rho(\mathbf{r}, t) = R(\mathbf{r}, t)^2$. With identification of the velocity as $\mathbf{v} = \nabla S / m$, and the flux as $\mathbf{j} = \rho \mathbf{v}$, equation (1) is the continuity equation. Hence, equations (1) and (2), arising from this so called Madelung transformation to the Schrödinger equation, have the form of classical hydrodynamic equations with the addition of an extra potential, often referred to as the *quantum* or *Bohm* potential, written as

$$Q = -\frac{\hbar^2}{2mR} \nabla^2 R \rightarrow -\frac{\hbar^2}{2m\sqrt{n}} \frac{\partial^2 \sqrt{n}}{\partial x^2}, \quad (3)$$

where the square root of the density n , represents the magnitude of the wave function R . The Bohm potential essentially represents a field through which the particle interacts with itself. It has been used, for example, in the study of wave packet tunneling through barriers [6], where the effect of the quantum potential is seen to lower or smooth barriers, and hence allow particles to leak through. A standard way to include quantum effects into classical simulation tools is to add the above-described quantum potential to the mean-field potential computed from solving Poisson's equation. Such potential corrections have been employed mostly in the context of fluid approximations leading to the so-called *quantum-hydrodynamic* (QHD) equations [7].

In analogy to the smoothed potential representations discussed for the QHD model above, it is desirable to define a smooth quantum potential for use in quantum particle based simulation. Ferry [8], based on the idea of Feynman and Kleinart [9], suggested an *effective potential* that is derived from a wave packet description of particle motion, where the extent of the wave packet is defined from the range of wavevectors established by the thermalized distribution function (specified via the carrier temperature). The effective potential seen by electrons is then represented as a convolution of the Hartree potential obtained from solving Poisson's equation and a Gaussian function. In other words,

$$V_{eff}(x) = \frac{1}{\sqrt{2\pi}a_0} \int_{-\infty}^{\infty} V(x') \exp\left(-\frac{(x-x')^2}{2a_0^2}\right) dx', \quad (4)$$

where $V(x)$ is the actual potential, and a_0 is the spatial spread of the wavepacket. The effective potential accounts for the *size of the electron* and its associated wavepacket, which feels the presence of barriers, etc. at a distance. From this Ansatz, the actual particle is treated as point-like in the presence of the effective potential associated with its wave-like nature, leading back to a classical particle simulation scheme. Since the additional simulation time needed to implement the aforementioned scheme is less than 10%, we have utilized the aforementioned approach in the existing 2D particle-based simulator to investigate the role of the quantum-mechanical space-quantization effects on the operation of a conventional 50 nm channel length MOSFET device and a 250 nm channel length FIBMOS device structure. Simulation results of these investigations are given in sections 2 and 3, respectively.

2 MOSFET SIMULATION RESULTS

The conventional 50 nm MOSFET device being simulated is schematically shown in Figure 2 and has channel doping of 10^{18} cm^{-3} , source/drain doping equal to 10^{19} cm^{-3} and junction depth of 36 nm. The oxide thickness is 2 nm

and the device width is $0.8 \mu\text{m}$, which requires simulation of approximately 30,000 electrons.

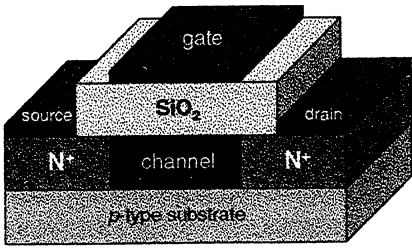


Figure 2: Schematics of the MOSFET device structure being simulated.

We find reduction in the electron density and charge set back by about 2 nm [10], in agreement with previous studies of this issue. These two factors give rise to threshold voltage reduction of $\sim 80 \text{ mV}$ and on-state current degradation of about 20%. Both trends are schematically shown in Figure 3, where we plot the device transfer and output characteristics, respectively. We note that, in order to get less noisy current measurements, when calculating the device transfer characteristics we use slightly higher drain bias ($V_D = 0.1 \text{ V}$) from what is used in the experiments. This is not a problem, however, since we are only interested in predicting the trends in the threshold voltage variation due to quantum-mechanical space-quantization effects.

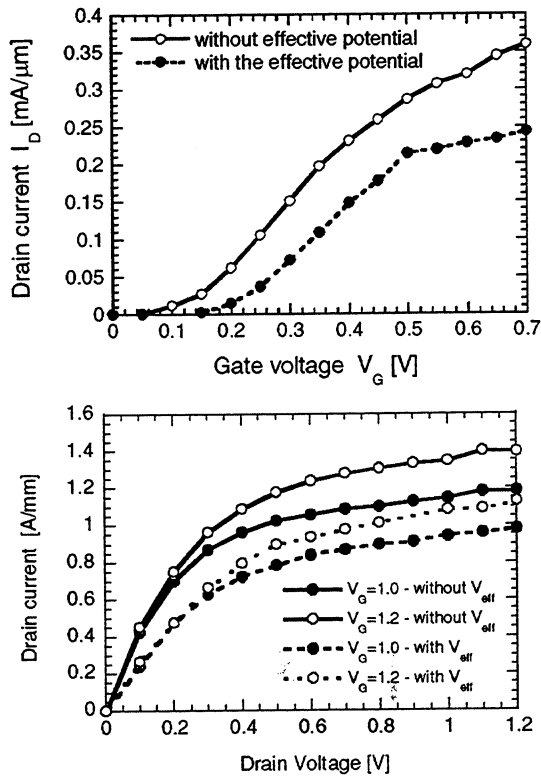


Figure 3: Top panel - Device transfer characteristics for $V_D = 0.1 \text{ V}$. Bottom panel: MOSFET output characteristics for two different values of the gate voltage.

3 FIBMOS SIMULATION RESULTS

In the design of ultra-small devices, one has to deal with two contradictory requirements: (1) the reduction of short-channel effects, that necessitate the use of high substrate doping densities, and (2) hot-carrier reliability increase and substrate current reduction, that require a reduction of the in-plane electric fields and, therefore, smaller substrate doping density. A device structure that satisfies both requirements must have asymmetric doping profiles, and there has been a vast amount of theoretical and experimental effort to predict optimal device structures that can operate reliably at higher drain voltages and do not exhibit pronounced short-channel effects. Some representative devices proposed include lightly-doped drain (LDD) devices, gate overlapped LDD structure (GOLD), halo source GOLD drain (HS-GOLD) [11] and graded-channel MOS (GCMOS) devices [12]. The last device structure overcomes the incompatible requirements of short-channel effects and hot-carrier resistance. As such, it is a rather promising way, in terms of reliability and performance, for downward scaling without the need to further reducing the power supply. Further improvements in this device structure have been made with the use of focused-ion-beam (FIB) implantation [13], that provides point by point control of the lateral dopant density at the source end of the channel, resulting in the so-called FIBMOS device structure.

A schematics of this last type of device structure being investigated in the present study is shown in Figure 4. The substrate doping equals 10^{16} cm^{-3} , source/drain doping is 10^{19} cm^{-3} , junction depth is 36 nm and bulk depth equals 400 nm . The oxide thickness is 5 nm and the width of the device being simulated is $1.4 \mu\text{m}$. The width of the FIB region is 70 nm , the depth equals the junction depth, and the doping is $1.6 \times 10^{18} \text{ cm}^{-3}$.

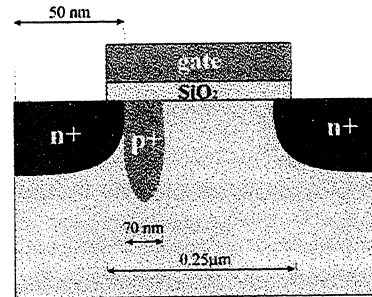


Figure 4: Schematic of the FIBMOS device being investigated.

As in the case of a conventional MOSFET device, in this device structure as well the quantization of charge in the inversion layer produces an expected increase of the threshold voltage in the channel. This observation is clearly seen from the results shown in the top panel of Figure 5, where we plot the linear drain current I_D as a function of the gate voltage V_G , for a drain voltage $V_D = 0.4 \text{ V}$. If we take as a criterion for determining the threshold voltage as being the gate voltage for which the drain current equals 10

$\mu\text{A}/\mu\text{m}$, we obtain a shift of approximately 200 mV when space-quantization effects are included in the model.

The device output characteristics are shown in the bottom panel of Figure 5. The four curves shown in this figure correspond to V_G equal to 1.0 V and 1.2 V, with and without V_{eff} . There are three noteworthy features in this figure: with V_{eff} , the drive current is reduced, the threshold voltage (V_{th}) is increased, and the transconductance is degraded. The inclusion of V_{eff} reduces the drain current I_D , due to two factors: the reduced average carrier velocity and the reduced sheet electron density, the latter being predominant. Also, since the slope of the I_D - V_D curve in the linear region is proportional to $V_G - V_{\text{th}}$, we see that for a given V_G the inclusion of V_{eff} increases V_{th} . Finally, if for a given V_D we analyze the current increase between V_G equal to 1.0 V and 1.2 V, which is (roughly) proportional to transconductance, it is clear that the transconductance is lower with V_{eff} included.

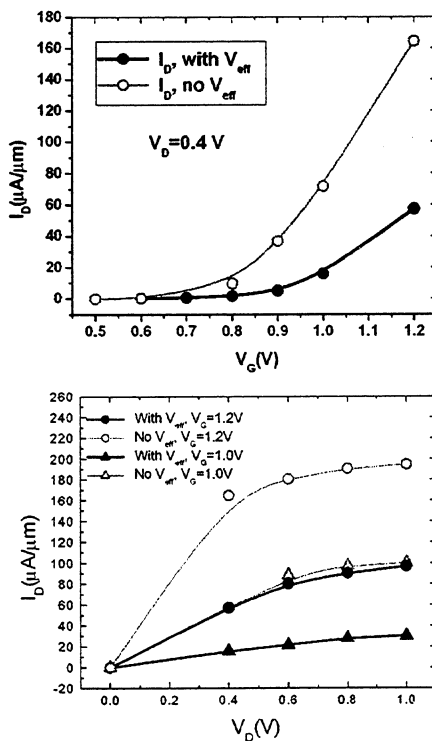


Figure 5: Top panel - transfer characteristics of a FIBMOS device. Bottom panel - output characteristics of a FIBMOS device.

4 CONCLUSIONS

In conclusion, we have investigated the role played by quantum-mechanical space-quantization effects on the operation of a 50 nm MOSFET device and a 250 nm FIBMOS device. We find threshold voltage shift between 100 and 200 mV and on-state current degradation between 20% and 40%, depending upon the bias conditions. These results suggest that it is crucial to include quantization effects into existing device simulators when trying to predict the per-

formance of state-of-the-art devices that exhibit very high substrate doping densities.

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