Scanning Tunneling Microscopy of Ultrathin Silicon-on-Insulator

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Summary. We present near-atomic-resolution scanning tunneling microscopy (STM) images of the surface of a 10 nm thick Si template layer in silicon-on-insulator (SOI), demonstrating that ultra-thin SOI, which is typically described as fully depleted of charge carriers, can indeed be imaged. We attribute the ability to image to our cleaning process, which results in a Si (001) free of oxide and defects. Electronic conduction in this type of very thin Si film is enabled by the interaction of Si (001) surface bands caused by the Si (001) 2x1 reconstruction with the bulk Si bands.

Silicon-on-insulator (SOI) has emerged as an important substrate for Si device technology, offering enhanced speed and reduced power consumption for field-effect transistors in comparison to conventional bulk-Si MOSFETs [1]. As the Si layer becomes very thin, interfaces begin to determine its electrical transport properties.

Usually the silicon template layer in SOI will be bounded by two SiO_2 layers, as the silicon template layer is covered either by native oxide or by gate oxide. The Si/SiO_2 interfaces play an important role in changing the film electronic properties. At a Si-SiO_2 interface, there exist charge trapping sites with energy levels within the bandgap (1.1eV). The interface trap density of states (D_{it}) typically exhibits a U shape across the Si band gap, with D_{it} of order $10^{11}cm^{-2}eV^{-1}$. Interface traps in the upper half of the band gap behave as acceptors, while those in the lower half behave as donors [2]. These interface charge traps arise from structural or oxidation–induced defects and are mainly in the form of Si “dangling bonds”.

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As the Si layer gets very thin, the interfaces will eventually deplete this layer of free carriers and the conductivity vanishes. To demonstrate this effect, we analyzed the sheet resistance of Si template layers with thicknesses ranging from 15nm to 200nm, sandwiched between a native oxide and the buried oxide, using the van der Pauw technique. We used Unibond™ SOI wafers from SOITEC, comprised of a silicon handle wafer, a 3μm buried oxide layer (BOX), and a 200 nm silicon top or “template” layer. Both the template and handle wafer are crystalline silicon with a (001) orientation, boron doped with a resistivity between 14-22 Ω-cm, corresponding to a carrier density of $\sim 10^{15}/cm^3$. We deliberately choose 3μm BOX to reduce the oxide leakage current. In order to obtain Si templates with different thicknesses, we thinned the top Si layer by dry thermal oxidation at 1050ºC, followed by wet chemical etching in HF. As shown in Figure 1, the measured sheet resistances are all higher than the resistance predicted for bulk Si for this nominal doping level. For Si template layer thicknesses below 30 nm, the sheet resistance ranged between $10^{10}\Omega$/square and $10^{11}\Omega$/square. Consistent with our prediction, holes in the film are getting trapped at the interfaces and the Fermi level is therefore pulled towards midgap.

Recent work using scanning tunneling microscopy (STM) concluded that SOI (001) with template layer thicknesses below ~35 nm is fully depleted, because the ability to create an image in STM ceased [3,4]. In contrast to these conclusions, we have been able to demonstrate STM imaging of the clean surface of SOI (001), with nominal doping level of $10^{15}/cm^3$ and Si template layers as thin as 10nm. The surface quality, rather than the Si thickness alone, dictates whether carrier density is high enough to enable STM imaging.

To investigate the clean Si (001) surface of SOI, the top oxide must be removed in ultrahigh vacuum (UHV). Surface preparation consists of *ex-situ* and *in-situ* cleaning. *Ex-situ*, the SOI is triple IMEC cleaned. A final piranha clean terminated the surface with a thin (1-2nm) protective surface oxide. The sample is then introduced into an ultrahigh-vacuum STM, which has a base pressure below $1x10^{-10}$ torr. Traditional *in-situ* preparation of bulk Si surfaces at 1500 K is not possible for ultra-thin SOI, because the Si template layer will dewet and agglomerate into 3D Si islands [5]. Instead, we deposit several monolayers of Si or Ge at 700°C, which reduce the surface SiO_2 to the volatile SiO or GeO. Finally we flash the sample to 800°C (still below the critical temperature for dewetting) for two minutes, quench it to and anneal it at 600°C for 30 minutes, radiation cool it, and then image it.

Figure 2 shows STM images of the clean SOI (001) surface. The 2x1 reconstruction via the formation of dimers occurs even for 10 nm thick Si template layers. The intrinsic anisotropic stress (tensile along the dimer bonds; compressive along the dimer rows) leads to the alternate orthogonal (2 x 1) and (1 x 2) terraces on the surface, terminated respectively by S_B and S_A steps. This dimerized surface leads to two-dimensional bands, a filled π band and an empty π^* band, separated by a ~0.5 eV gap [6]. The density of states in the two-dimensional bands is around 10^{15} $cm^{-2}eV^{-1}$. Our low-thermal-budget surface cleaning method allows us to remove the protective oxide without breaking up the fragile Si template layer and produces very-low-defect-density surfaces. The fact that we can image very thin SOI in STM implies that the depletion of the thin Si layer is not important. Admittedly only one surface is now covered with oxide, but the trap states at this one interface are more than sufficient to maintain the full bulk depletion of the Si layer. It is the presence of the surface bands due to the dimer reconstruction that enables the conduction necessary to image the surface in STM. It is not, however, the conduction through the surface bands directly that makes the film conduct, as one might at first imagine. It is the position in energy of the surface bands relative to the bulk bands, and the high density of states in the bulk valance band and the surface conduction band that enables the conduction [7]. The bulk doping density and the density of interface states on the back Si/SiO_2 interface are largely irrelevant for electronic transport in ultrathin template layers in SOI with a clean reconstructed surface.

In summary, we show that STM imaging of the clean surface of SOI (001) with nominal doping levels of $10^{15}/cm^3$ and silicon template layers as thin as 10 nm is entirely possible, even though such films are depleted of charge carriers and should behave like intrinsic Si. The surface bands caused by reconstruction enable electronic transport. We predict that only disruption of the surface bands can hinder imaging of SOI (001), no matter how thin the Si film is or how low the bulk doping level is. Such disruption can come via surface disorder or chemisorption that in Si (001) breaks the pi-bonded dimer chains that produce the surface bands. In systems that do not have surface bands, we predict that making the layer thin enough to cause bulk depletion will inhibit imaging. Moreover, we believe our surface cleaning method with low thermal budget should be applicable to actual device fabrication, because the same deposition technique and source material can be used both to clean and to grow epitaxial layers for raised source and drain [8], as well as to image the surface with STM and perform other electron-transport-dependent measurements.

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Fig. 1. Sheet resistance measured from van der Pauw method versus film thickness (circles with error bars). The solid curve is the predicted sheet resistance calculated from the nominal bulk doping density (10^{15}/cm^3).

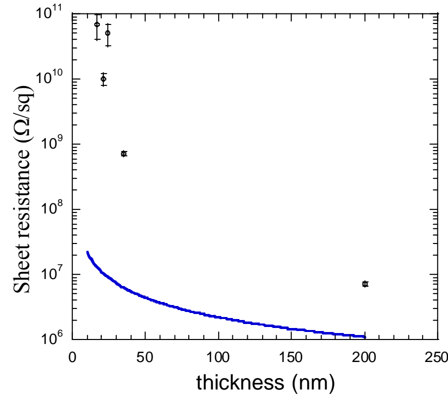
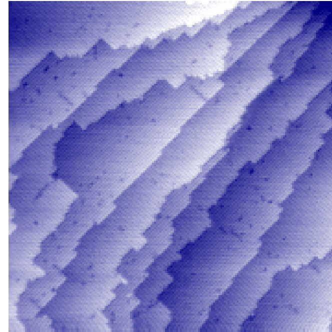


Fig. 2. Filled-state STM image of the surface of a 10nm thick Si template layer of bonded SOI (001) with native oxide removed by 3 ML of Ge. V_{sample} = -2V, 100 nm x 100 nm view.



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