Electron Mobility in Silicon Nanowires

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***Abstract*—The low-field electron mobility in rectangular silicon nanowire (SiNW) transistors was computed using a self-consistent Poisson–Schrödinger–Monte Carlo solver. The behavior of the phonon-limited and surface-roughness-limited components of the mobility was investigated by decreasing the wire width from 30 to 8 nm, the width range capturing a crossover between two-dimensional and one-dimensional electron transport. The phonon-limited mobility, which characterizes transport at low and moderate transverse fields, is found to decrease with decreasing wire width due to an increase in the electron–phonon wavefunction overlap. In contrast, the mobility at very high transverse fields, which is limited by surface roughness scattering, increases with decreasing wire width due to volume inversion. The importance of acoustic phonon confinement is also discussed briefly.**

***Index Terms*—Electron mobility, silicon nanowires, surface roughness.**

I. Introduction

A KEY FACTOR behind the growth of the semiconductor industry for the past 40 years has been the continuous scaling of the device dimensions to obtain higher integration and performance gain. According to the International Technology Roadmap for Semiconductors (ITRS) 2005, the scaling of CMOS technology will continue for at least another decade [1]. Scaling trends also indicate that the devices of the next decade will be quasi-one-dimensional (Q1D) nanowires (NW) with spatial confinement along two directions. Due to the compatibility with the existing fabrication facilities, and the superior performance of silicon-on-insulator (SOI) based MOSFETs [2], ultranarrow SOI NWs are expected to play a critical role in future technology nodes. Therefore, it is crucial to accurately model and estimate the performance of these devices.

The low-field electron mobility is one of the most important parameters that determine the performance of a field-effect transistor. Due to the reduced density of states for scattering in one-dimensional (1-D) structures, the electron mobility in nanowires is expected to increase significantly [3]. Some experimentalists [4], [5] claim to have observed such enhancement of electron mobility in SiNW FETs. But Kotlyar *et al.* [6] have shown that, in a cylindrical SiNW, the phonon-limited mobility decreases with decreasing diameter due to an increased overlap between the electron and phonon wavefunctions. Recent work also shows that surface roughness scattering (SRS) becomes less important in ultrasmall SiNWs [7].

In this work, we investigate the mobility of electrons in a rectangular SiNW by taking into account electron scattering due to acoustic phonons, intervalley nonpolar optical phonons, and imperfections at the Si–SiO_2 interface, and also discuss the importance of incorporating the confinement of acoustic phonons in these structures. Section II describes the device structure used in this study and the components of the simulator employed to calculate the mobility. The simulation results are presented in Section III, while concluding remarks and a brief summary are presented in Section IV.

II. Device Structure and Mobility Calculation

The structure considered in this work is a long, narrow SiNW on ultrathin SOI, similar to the channel of the device depicted in Fig. 1 that was originally proposed by Majima *et al.* [8]. This ultranarrow SOI MOSFET has a 700-nm silicon substrate, an 80-nm buried oxide, an 8-nm-thick SOI layer and a 25-nm gate-oxide. The width of the SiNW in the present simulation is varied from 30 to 8 nm, and the channel doping is uniform at 3×10^{15} cm^{-3}. A schematic of the device and the potential profile along the cutline CC', obtained by self-consistently solving the two-dimensional (2-D) Poisson and 2-D Schrödinger equations, are shown in Fig. 1. The large wire length enables us to approximate it as infinite in the direction of the current flow, so only the carriers' lateral momenta (and not their positions) need to be updated in the Monte Carlo kernel. The long wire also implies that transport is diffusive (the length exceeds carrier mean free path), which justifies the use of semiclassical Monte Carlo simulation.

As mentioned before, only phonon scattering and SRS are considered in this work. SRS was modeled using Ando's model [9], and the phonons were treated in the bulk mode approximation. Since the wire is very lightly doped, the effect of impurity scattering was not included. A nonparabolic band model for silicon, with nonparabolicity factor $\alpha = 0.5$ eV^{-1}, was used in the calculation of the scattering rates. The details of the simulator and the derivation of 1-D scattering rates can be found in [10]; here, we present only the final expressions used for the scattering rates calculation.

The intravalley acoustic phonon scattering rate, assuming elastic scattering and the equipartition approximation, is given by

$$\Gamma^{\mathrm{ac}}_{nm}(k_x) = \frac{\Xi^2_{\mathrm{ac}} k_B T \sqrt{m^*}}{\sqrt{2}\hbar^2 \rho \upsilon^2} \mathcal{D}_{nm} \frac{(1+2\alpha\mathcal{E}_f)}{\sqrt{\mathcal{E}_f(1+\alpha\mathcal{E}_f)}} \Theta(\mathcal{E}_f) \quad (1)$$

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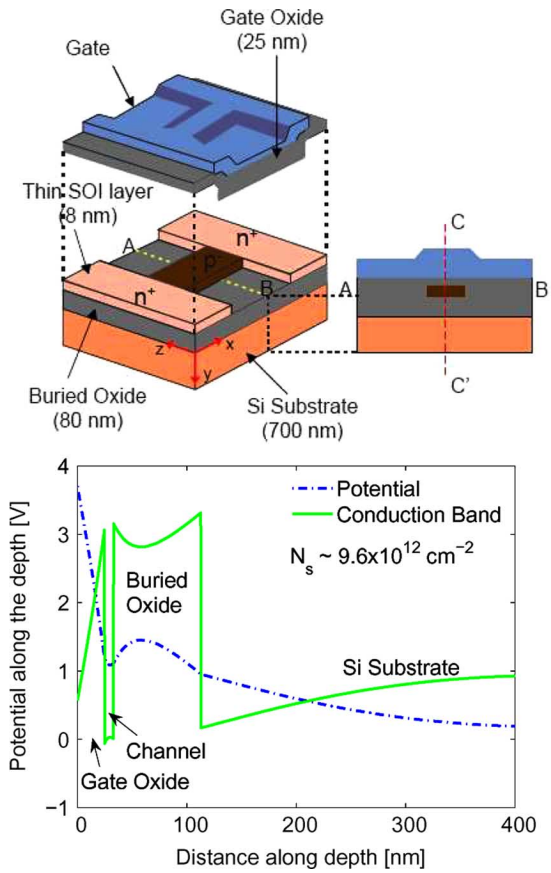

Fig. 1. The top panel shows the schematic of the simulated SiNW on ultrathin SOI. The conduction band profile depicted in the bottom panel is taken along the red cutline CC' from the top panel. The width of the channel is 30 nm.

where $\Xi_{\rm ac}$ is the acoustic deformation potential, ρ is the crystal density, and v is the sound velocity. n and m are the initial and final subband index, respectively, while $\mathcal{E}_n$ and $\mathcal{E}_m$ are the corresponding subband energies. k_x is the initial wavevector in the x direction, in which the motion is unconfined; $\mathcal{E}_{k_x}$ is the initial (parabolic) kinetic energy associated with k_x; and $\mathcal{E}_f$ is the final kinetic energy, given by

$$\mathcal{E}_{k_x} = \frac{\hbar^2 k_x^2}{2m^*}, \tag{2a}$$

$$\mathcal{E}_f = \mathcal{E}_n - \mathcal{E}_m + \frac{\sqrt{1+4\alpha\mathcal{E}_{k_x}}-1}{2\alpha}. \tag{2b}$$

$\mathcal{D}_{nm}$ represents the electron–phonon wavefunction overlap integral [6], given by

$$\mathcal{D}_{nm} = \int\int |\psi_n(y,z)|^2 |\psi_m(y,z)|^2 \, dy\, dz \tag{3}$$

where $\psi_n(y,z)$ and $\psi_m(y,z)$ are the electron wavefunctions in subbands n and m, respectively.

The intervalley nonpolar optical phonon scattering rate is given by

$$\Gamma^{\rm op}_{nm}(k_x) = \frac{\Xi^2_{\rm op}\sqrt{m^*}}{2\sqrt{2}\hbar\rho\omega_0}\left(N_0+\frac{1}{2}\pm\frac{1}{2}\right)\mathcal{D}_{nm} \times\frac{(1+2\alpha\mathcal{E}_f)}{\sqrt{\mathcal{E}_f(1+\alpha\mathcal{E}_f)}}\Theta(\mathcal{E}_f) \tag{4}$$

where $\Xi_{\rm op}$ is the optical deformation potential, and $\mathcal{D}_{nm}$ is defined in (3). The approximation of dispersionless bulk optical phonons of energy $\hbar\omega_0$ was adopted, where $N_0 = [\exp(\hbar\omega_0/k_BT)-1]^{-1}$ is their average number at temperature T. The Heaviside step function $\Theta(\mathcal{E}_f)$ ensures the conservation of energy after scattering, so the final kinetic energy $\mathcal{E}_f$ in the case of optical phonons is similar to that in the acoustic phonon expression (2b), but with an additional $\mp\hbar\omega_0$ on the right-hand side to account for the emission/absorption of a phonon of energy $\hbar\omega_0$.

Assuming exponentially correlated surface roughness [11] and incorporating the wavefunction deformation using Ando's model [9], the SRS rate is given by

$$\Gamma^{\rm sr}_{nm}(k_x,\pm) = \frac{4\sqrt{m^*}e^2}{\hbar^2}\frac{\Delta^2\Lambda}{2+(q_x^{\pm})^2\Lambda^2}|\mathcal{F}_{nm}|^2 \times\frac{(1+2\alpha\mathcal{E}_f)}{\sqrt{\mathcal{E}_f(1+\alpha\mathcal{E}_f)}}\Theta(\mathcal{E}_f) \tag{5}$$

where $\mathcal{E}_f$ is given by (2b), and Δ and Λ are the rms height and the correlation length of the fluctuation at the Si–SiO_2 interface, respectively. To fit the experimental data, $\Delta = 0.45$ nm and $\Lambda = 2.5$ nm are used in this work to characterize the SRS due to each of the four interfaces. $q_x^{\pm} = k_x - k_x'$ is the transferred wavevector, where the angle between the initial (k_x) and the final (k_x') electron wavevector can only be 0 or π, corresponding to the $\pm$ in the superscript. The SRS overlap integral in (5), for the top and bottom interface, is given by

$$\mathcal{F}_{nm} = \int\int dy\, dz\left[\psi_m(y,z)\mathcal{E}_m\frac{\partial\psi_n(y,z)}{\partial y} + \psi_n(y,z)\varepsilon_y(y,z)\psi_m(y,z) + \psi_n(y,z)\mathcal{E}_n\frac{\partial\psi_m(y,z)}{\partial y}\right]. \tag{6}$$

The SRS rate and its corresponding overlap integral for the two side interfaces can be obtained by interchanging y and z in (6).

Using the wavefunctions and potential obtained from the self-consistent Poisson–Schrödinger solver, the scattering rates are calculated. The phonon deformation potentials were taken from [12]. A Monte Carlo transport kernel [13] is used to model electron transport in the unconfined x direction under the influence of a very low lateral electric field. The mobility of the electrons in the channel is then calculated from the ensemble average of the electron velocities [13].

III. Simulation Results

A. Validation of the Simulator

A device with a width of 30 nm [at this width, electrons in the channel feel very weak spatial confinement along the width direction and therefore behave like a 2-D electron gas (2DEG)] was used to compare the mobility results obtained from our simulator with the experimental data of Koga *et al.* [14] for a 2DEG of the same thickness. Fig. 2 shows the calculated low-field electron mobility variation with the transverse effective field. Although there is a good agreement with the experimental data at high fields, we find that the simulator overestimates the mobility in the moderate and low-field regions, where phonon scattering

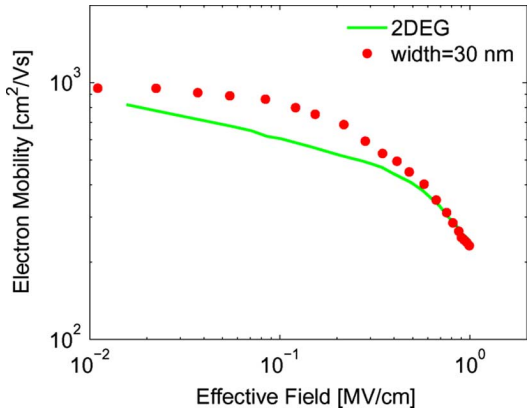

Fig. 2. Low-field mobility in a 30-nm-wide SiNW as a function of the effective transverse field, as obtained from the simulation (filled circles) and the experiment of Koga *et al.* [14] for a 2DEG (solid line).

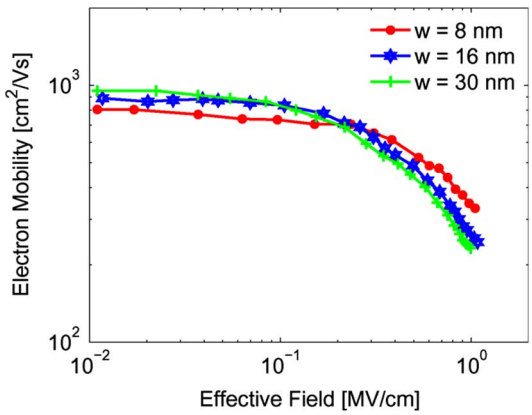

Fig. 3. Variation of the field-dependent mobility with varying SiNW width. The wire thickness is kept constant at 8 nm.

dominates. This discrepancy is due to the bulk phonon approximation used in the calculation of the electron–phonon scattering rates, and a similar result has been reported in ultrathin SOI structures [15], [16]. The importance of including phonon confinement in the calculation of the electron–phonon scattering rates in nanostructures has previously been established [17], [18]. In ultrathin and ultranarrow structures, the phonon spectrum is modified due to the mismatch of the sound velocities and dielectric constants between the wire and the surrounding material [19], [20], in our case—silicon and SiO_2. Presently, we are working on incorporating confined acoustic phonons in the calculation of electron–phonon scattering rates in SiNWs, and the results will be presented in a subsequent publication. Even for a relatively wide, 30-nm wire, preliminary results indicate that the acoustic phonon scattering rate is significantly higher when phonon confinement is included in the calculation.

B. *Effect of Decreasing Channel Width*

The variation of the field-dependent mobility with decreasing channel width was investigated on a series of SiNWs, while keeping the channel thickness at 8 nm. Fig. 3 shows the mobility for SiNWs with the widths of 30, 16, and 8 nm. Two important results regarding the mobility behavior in the width range considered can be deduced from Fig. 3: 1) the mobility at high transverse fields, which is dominated by SRS, increases with decreasing wire width and 2) the mobility at low-to-moderate

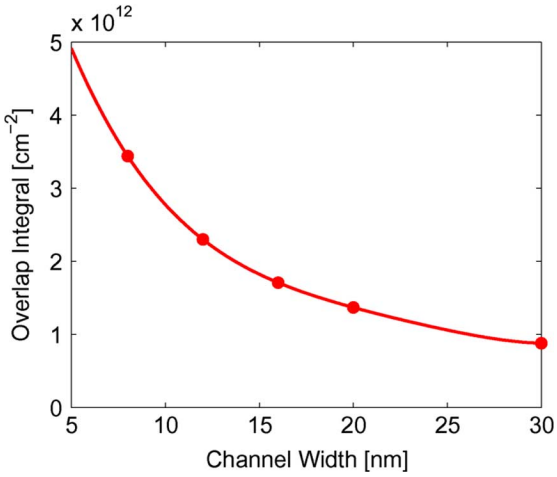

Fig. 4. Variation of the overlap integral for the lowest subband with varying wire width, obtained from (3) at a constant sheet density of $N_s = 2.9 \times 10^{11}$ cm^{-2}.

transverse fields, determined by phonon scattering, decreases with decreasing wire width.

1) Effect of Bulk Phonon Scattering: Phonon scattering variation with decreasing wire width is determined by the interplay of two opposing factors: 1) reduction of the final density of states for the electrons to scatter to and 2) an increase in the electron–phonon wavefunction overlap (3). The former results in an enhanced mobility, while the latter results in mobility degradation. The overlap integral (3) shown in Fig. 4 for various widths increases with a decrease in the wire width due to an increase in the electron confinement. In narrow wires, the increase in the electron–phonon wavefunction overlap dominates over the density-of-states reduction, resulting in a net decrease in the electron mobility at low-to-moderate transverse fields.

2) Effect of SRS: The SRS overlap integral given by (6) has three terms. Two are due to deformation of the wavefunction, and the third, dominant term depends on the strength of the field perpendicular to the interface. Since the field normal to the side interfaces is very weak, SRS due to these interfaces is much less efficient than scattering due to the top and bottom ones. The decrease in SRS with decreasing wire width can be understood by following the behavior of the average distance (7) of the carriers from the top interface

$$\langle y \rangle = \frac{1}{N_l} \sum_{i,\nu} N_l^{i,\nu} \int\int |\psi_i^{\nu}(y,z)|^2 y \, dy \, dz \qquad (7)$$

where N_l is the total line density and $N_l^{i,\nu}$ is the line density in the ith subband of the νth valley. In Fig. 5, we can see that the carriers are moving away from the top interface as the width of the wire is decreased, and are therefore not strongly influenced by the interface. This behavior is also observed in the case of ultrathin double-gate SOI FETs, and is due to the onset of volume inversion [21], [22]. As the SiNW approaches the volume inversion limit, carriers cease to be confined to the interfaces, but are distributed throughout the silicon volume. Fig. 6 shows the distribution of carriers in a 30-nm wire and a 8-nm wire at the same effective field; we can clearly see that the carriers are confined extremely close to the interface in the 30-nm-wide wire,

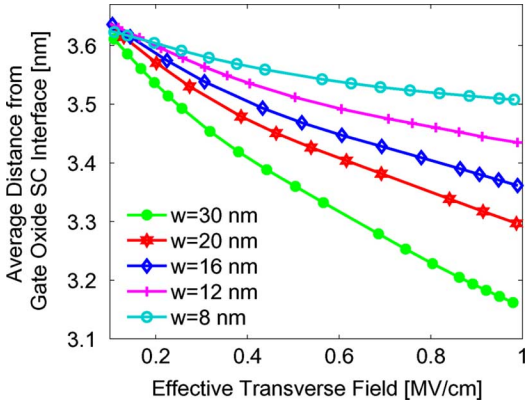

Fig. 5. Variation of the average distance of carriers from the top interface (below the gate) for various wire widths as a function of the effective transverse field.

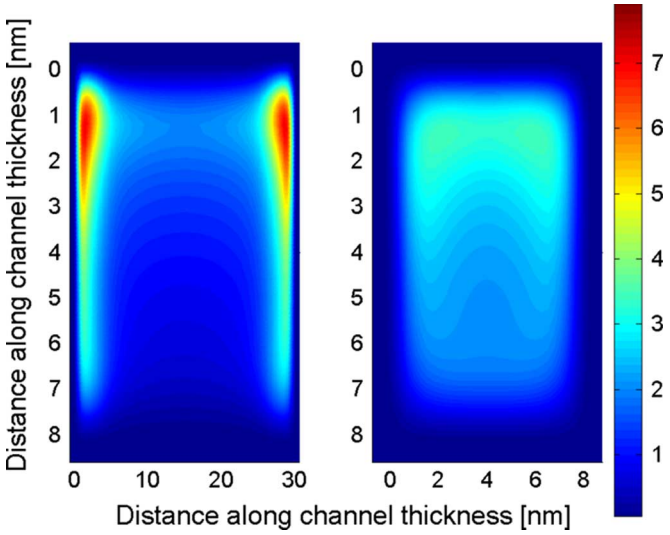

Fig. 6. Electron distribution across the nanowire, for the wire width of 30 nm (left panel) and 8 nm (right panel). In both panels, the transverse field is 1 MV/cm, the wire thickness is 8 nm, and the color scale is in $\times 10^{19}$ cm^{-3}.

whereas they are distributed throughout the silicon layer in the case of the 8-nm wire.

IV. Conclusion

The transverse-field dependence of the low-field electron mobility in rectangular silicon nanowires was calculated using a self-consistent 2-D Poisson–Schrödinger–1D Monte Carlo simulation. The effects of varying the wire width and the relative importance of phonon scattering and SRS were investigated. For widths in the range between 30 and 8 nm, the phonon-limited mobility (dominant at low to moderate transverse fields) was found to decrease with decreasing nanowire width, because of the increase in the electron–phonon wavefunction overlap. SRS was found to decrease with decreasing width due to volume inversion. At high transverse fields, volume inversion results in an appreciable mobility enhancement.

References

[1] "Emerging research devices" Jun. 2006 [Online]. Available: http://www.itrs.net/common/2005ITRS/Home2005.htm, ITRS 2005 Edition

[2] J. P. Colinge, *Silicon-On-Insulator Technology: Materials to VLSI*. Boston, MA: Kluwer, 1991.

[3] H. Sakaki, "Scattering suppression and high-mobility effect of size-quantized electrons in ultrafine semiconductor wire structures," *Jpn. J. Appl. Phys.*, vol. 19, no. 12, pp. L735–L738, 1980.

[4] Y. Cui, Z. H. Zhong, D. L. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149–152, 2003.

[5] S. M. Koo, A. Fujiwara, J. P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, "High inversion current in silicon nanowire field effect transistors," *Nano Lett.*, vol. 4, no. 11, pp. 2197–2201, 2004.

[6] R. Kotlyar, B. Obradovic, P. Matagne, M. Stettler, and M. D. Giles, "Assessment of room-temperature phonon-limited mobility in gated silicon nanowires," *Appl. Phys. Lett.*, vol. 84, no. 25, pp. 5270–5272, 2004.

[7] J. Wang, E. Polizzi, A. Ghosh, S. Datta, and M. Lundstrom, "Theoretical investigation of surface roughness scattering in silicon nanowire transistors," *Appl. Phys. Lett.*, vol. 87, no. 4, p. 043 101, 2005.

[8] H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental evidence for quantum mechanical narrow channel effect in ultra-narrow MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 396–398, Aug. 2000.

[9] T. Ando, A. B. Fowler, and F. Stern, "Electronic propeties of two-dimensional systems," *Rev. Mod. Phys.*, vol. 54, no. 2, pp. 437–672, 1982.

[10] E. B. Ramayya, "Modeling of mobility in a rectangular silicon nanowire transistor," M.S. thesis, Arizona State Univ., Tempe, May 2006.

[11] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, "Surface roughness at the Si(100)-SiO2 interface," *Phys. Rev. B*, vol. 32, no. 12, pp. 8171–8186, 1985.

[12] S. Takagi, J. Koga, and A. Toriumi, "Mobility enhancement of SOI MOSFETs due to subband modulation in ultrathin SOI films," *Jpn. J. Appl. Phys.*, vol. 37, no. 3B, pp. 1289–1294, 1998.

[13] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Rev. Mod. Phys.*, vol. 55, no. 3, pp. 645–705, 1983.

[14] J. Koga, S. Takagi, and A. Toriumi, "Influences of buried-oxide interface on inversion-layer mobility in ultrathin SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1042–1048, Jun. 2002.

[15] L. Donetti, F. Gamiz, J. B. Roldan, and A. Godoy, "Acoustic phonon confinement in silicon nanolayers: Effect on electron mobility," *J. Appl. Phys.*, vol. 100, no. 1, p. 013 701, 2006.

[16] L. Donetti, F. Gamiz, N. Rodriguez, F. Jimenez, and C. Sampedro, "Influence of acoustic phonon confinement on electron mobility in ultrathin silicon on insulator layers," *Appl. Phys. Lett.*, vol. 88, no. 12, p. 122 108, 2006.

[17] S. Yu, K. W. Kim, M. A. Stroscio, G. J. Iafrate, and A. Ballato, "Electron-acoustic-phonon scattering rates in rectangular quantum wires," *Phys. Rev. B*, vol. 50, no. 3, pp. 1733–1738, 1994.

[18] A. Svizhenko, S. Bandyopadhyay, and M. A. Stroscio, "The effect of acoustic phonon confinement on the momentum and energy relaxation of hot carriers in quantum wires," *J. Phys., Condens. Matter*, vol. 10, pp. 6091–6104, 1998.

[19] E. P. Pokatilov, D. L. Nika, and A. A. Balandin, "Acoustic phonon engineering in coated cylindrical nanowires," *Superlattices Microstruct.*, vol. 38, no. 3, pp. 168–183, 2005.

[20] E. P. Pokatilov, D. L. Nika, and A. A. Balandin, "Acoustic-phonon propagation in rectangular semiconductor nanowires with elastically dissimilar barriers," *Phys. Rev. B*, vol. 72, p. 113 311, 2005.

[21] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion—A new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. 8, no. 9, pp. 410–412, Sep. 1987.

[22] F. Gamiz and M. V. Fischetti, "Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5478–5487, 2001.

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