

Lin Xie

CONTACT INFORMATION	Dept. of Electrical & Computer Engineering University of Wisconsin - Madison 4616 Engineering Hall Madison, WI 53706 USA	<i>Voice:</i> (608) 628-7987 <i>Email:</i> lxie2@wisc.edu <i>Homepage:</i> www.cae.wisc.edu/~lxie
OBJECTIVE	Co-op/intern position in computer-aided design for integrated circuits for summer 2009	
RESEARCH INTERESTS	Statistical modeling and optimization; post-silicon timing failure diagnosis and repair; physical synthesis under variation; test for variability; parallel optimization for computer-aided design.	
EDUCATION	University of Wisconsin , Madison, WI USA Ph.D., Electrical and Computer Engineering <ul style="list-style-type: none">• Advisor: Prof. Azadeh Davoodi; <i>Area: Computer Engineering</i> M.S., Industrial and Systems Engineering <ul style="list-style-type: none">• Advisor: Prof. Vicki Bier; <i>Area: Operations Research & Decision Science</i> Zhejiang University , Hangzhou, China M.S., Electrical Engineering, Mar. 2006 B.S., Electrical Engineering, Jun. 2003	
ACADEMIC EXPERIENCE	Dept. of ECE, University of Wisconsin , Madison, WI <i>Ph.D. Candidate</i> Jan. 2007 to present <ul style="list-style-type: none">• Input-Vector Dependent Timing Yield Estimation Under Variations Proposed an accurate timing yield estimation approach, which incorporates vector-dependent gate delay models, both static and dynamic false paths under process variation• Critical Path Extraction Under Variability Proposed an exact and fast bound-based algorithm to extract top critical paths under process variation, which can be applied for physical synthesis under variations and at-speed test• Statistical Static Timing Analysis with High Dimension of Variability Developed an adjustment-based framework for statistical static timing analysis with high dimension of variability, which is distribution free and can be easily parallelized• Robust Timing Yield Estimation with Partial Information on Process Variation Applied distributional robustness theory to compute worst-case timing yield when partial statistical information on process variation is known; Obtained appropriate conditions to incorporate within-die/die-to-die variations• Statistical Static Timing Analysis with Non-Gaussian Process Variation Developed a fast and accurate statistical static timing analysis scheme to handle skewed process variation. The obtained scheme can be 1000X faster than Monte Carlo based statistical static timing analysis approach	

Dept. of ECE, Texas A&M University, College Station, TX

Graduate Student

Aug. 2006 to Dec. 2006

- Quality-of-Service for Mobile Networking
Proposed several opportunistic cooperation strategies for quality of service provisioning under time/frequency division multiple access mechanisms

Dept. of ISEE, Zhejiang University, Hangzhou, China

Master Student

Sept. 2003 to Mar. 2006

- Low Power Bus Coding for Deep Submicron Technology
Proposed a new partitioned bus coding scheme based on transition pattern coding to reduce the energy consumption
- Cooperative Diversity for Wireless Communication
Proposed relay selection strategies for distributed cooperative systems

MAIN COURSES
TAKEN AT
UW-MADISON

Introduction to Computer Architecture; Advanced Computer Architecture; Digital VLSI Circuit Design; Design Automation for Digital Systems; CAD for VLSI; Nonlinear Optimization; Optimization Modeling; Stochastic Modeling Technique; Simulation Modeling & Analysis; Stochastic Process & Queueing Theory; Introduction to Decision Science.

ACADEMIC DESIGN
PROJECTS AT
UW-MADISON

Pipelined Processor: Investigated the application of elastic pipeline in handling variable latency cache access. Specifically, we consider different cache access time due to cache location and process variation

Pipelined Processor: Designed a 16-bit pipelined processor with 2 way set-associative cache. Implemented features including data forwarding and branch prediction

ALU Design: Used Cadence commercial tools (Spectre and Virtuoso) to design and layout a 16-bit ALU with its periphery circuits

TECHNICAL SKILLS

IC design tools: Cadence Spectre, Virtuoso, Encounter, Synopsys Design Compiler
Simulation tools: Matlab, R, Mathematica, Simplescalar, PUFF
Programming language: C/C++, GAMS, Verilog HDL
Operating system: Windows, Unix/Linux

JOURNAL
PUBLICATIONS

L. Xie, A. Davoodi, and K.K. Saluja, "False path aware timing yield estimation," submitted to *IEEE Trans. Very Large Scale Integr. Syst. (TVLSI)*, 2009

L. Xie, A. Davoodi, J. Zhang, and T.-H Wu, "Adjustment-based modeling for statistical static timing analysis with high dimension of variability," under revision in *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. (TCAD)*, 2008

L. Xie, and A. Davoodi, "Robust estimation of timing yield with partial statistical information on process variations," in *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. (TCAD)*, Dec. 2008

T.-H. Wu, **L. Xie**, and A. Davoodi, "A parallel and randomized algorithm for large-scale discrete dual-Vt assignment and continuous gate sizing," in *ASP Journal of Low Power Electronics (JLOPE)*, Aug. 2008

L. Xie, and A. Davoodi, "Fast and accurate statistical static timing analysis with skewed process parameter variation," in *IET Circuits, Devices & Systems*, Apr. 2008

L. Xie, L. Yu, and P. Qiu, "Research on context-based adaptive arithmetic coding," in *Journal of Zhejiang University (Engineering)*, Jun. 2005. (Printed in Chinese)

SELECTED
CONFERENCE
PUBLICATIONS

L. Xie, A. Davoodi, K.K. Saluja, and A. Sinkar “Vector-dependent timing-yield estimation under variations,” in *IEEE VLSI Test Symp. (VTS)*, May 2009

L. Xie, and A. Davoodi, “Bound-based identification of timing-violating paths under variability,” in *IEEE/ACM Asia South-Pacific Des. Autom. Conf. (ASP-DAC)*, Jan. 2009

L. Xie, and A. Davoodi, J. Zhang, and T.-H Wu, “Adjustment-based modeling for statistical static timing analysis with high dimension of variability,” in *IEEE/ACM Int. Conf. Comput.-Aided Des. (ICCAD)*, Nov. 2008

T.-H. Wu, **L. Xie**, and A. Davoodi, “A parallel and randomized algorithm for large-scale discrete dual-Vt assignment and continuous gate sizing,” in *IEEE/ACM Int. Symp. Low Power Electron. Des. (ISLPED)*, Aug. 2008

L. Xie, and A. Davoodi, “Fast and accurate statistical static timing analysis with skewed process parameter variation,” in *IEEE/ACM Int. Symp. Qual. Electron. Des. (ISQED)*, Mar. 2008

L. Xie, and A. Davoodi, “Robust estimation of timing yield with partial statistical information on process variations,” in *IEEE/ACM Int. Symp. Qual. Electron. Des. (ISQED)*, Mar. 2008

J. Lee, **L. Xie**, and A. Davoodi, “A dual-Vt low leakage SRAM array robust to process variations,” in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2008

L. Xie, P. Qiu, and Q. Qiu, “Partitioned bus coding for energy reduction,” in *IEEE/ACM Asia South-Pacific Des. Autom. Conf. (ASP-DAC)*, Jan. 2005

Please refer to my homepage for a full list of my publications.

HONORS AND
AWARDS

Travel Grant from Office of Naval Research, 2007

Travel Grant from National Science Foundation(NSF)/ACM-SIGDA, 2007, 2008

ACM-SIGDA Young Student Scholarship at Design Automation Conference, 2007

Samsung Scholarship (granted to top 0.5% students), Zhejiang University, 2005

Excellent Student, Zhejiang University, 2000, 2001, 2005, 2006

School Academic Scholarship, Zhejiang University, 2000, 2001, 2002, 2005

Best B.S. Thesis Award (granted to 2/89 in the major), Zhejiang University, 2003

PROFESSIONAL
EXPERIENCE

Reviewer:

IEEE Transactions on Wireless Communication

EURASIP Journal on Wireless Communications and Networking

IEEE Conferences: DAC, ISQED, ISLPED, ICC, WCNC, GLOBECOM, and et al.

Referee:

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

IEEE Conferences: ICCAD, DATE, ICCD, VLSID, GLSVLSI, INFOCOM, and et al.

REFERENCE

Available upon request.