Mikko Lipasti
Fall 2005

ECE/CS 552: Introduction to Computer Architecture
ASSIGNMENT #1
Due Date: In class September 21st, 2005

This homework is to be done individually. Total 4 Questions, 75 points

1. **(15 Points – 3 each)**
   a. Problem 2.1 from Text.
   b. Problem 2.2 from Text.
   c. Problem 2.3 from Text.
   d. Problem 2.4 from Text.
   e. Problem 2.5 from Text.
2. **(10 points)** Assume the following instruction mix for a MIPS-like RISC instruction set: 15% stores, 20% loads, 25% branches, and 30% integer arithmetic, 5% integer shift, and 5% integer multiply. Given a program with 200 instructions and that load instructions require two cycles, branches require 4 cycles, integer ALU and store instructions require one cycle and integer multiplies require 10 cycles, compute the overall cycles-per-instruction or CPI.
3. **(10 points)** Strength reduction is common compiler optimization that converts multiplies by a constant integer into a sequence of shift and add instructions with equivalent semantics. Given the same parameters of problem 2, consider such a strength-reducing optimization that converts multiplies by a compile-time constant into a sequence of shifts and adds. For this instruction mix, 50% of the multiplies can be converted into shift-add sequences with an average length of 3 instructions. Assuming a fixed frequency, compute the new CPI and overall program speedup.
4. **(10 points)** Assume a particular function in the latest 3D game contains 1 million instructions, breaking down into the following: 15% stores, 15% loads, 30% branches, 10% integer arithmetic and 30% floating point operations. Given a personal computer running at 3.0 Ghz and that load and arithmetic instructions require one cycle, stores require two cycles, branches require four cycles and floating point instructions requires ten cycles, how long will it take for this particular function to finish (in milliseconds)?
5. **(25 points)** *Mentor Graphics Design and Simulation*

Using Mentor Graphics Design Architect, design a logic unit that takes two 16-bit inputs (A and B) and based on two control signals (C1 and C2), performs one of four Boolean expressions and then outputs the result on a 16-bit output (Z). The functionality of this device shall be defined as such:

C1	C2	Output	Operation
0	0	Z = A AND B	AND
0	1	Z = A OR B	OR
1	0	Z = A XOR B	XOR
1	1	Z = INV(A)	NOT

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You should turn in the following :

1. A Design Architect Schematic of your Logic Unit.
2. A QuickSim II Force File used to test your Logic Unit.
3. An output from the list window showing simulation results corresponding to your force file. **Be sure to show that all four functions work correctly.**