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Fall 2005

ECE/CS 552: Introduction to Computer Architecture
ASSIGNMENT #3
Due Date: In class October 19th, 2005

This homework is to be done individually. Total 4 Questions, 90 points

General Instructions:

All gates must have four or fewer inputs. Set the **RISE and FALL** of each gate in the design equal to **(#of inputs) ns**. Delays of an invertor,"buf.3so","buf", "buf.3so.n", "buf.n" are 2ns.You can change a component delay by placing the mouse pointer on the current/default delay value and typing ***shift* F7. Note:** To simulate your design with the new delays you must use the **timing_mode typ** option when starting QuickSim II. Otherwise the delays won't take effect in the simulation.
For example:
sun-xx% **quicksim –timing_mode typ** design_name

1. (15 points - 5 points each)
Using the standard IF-ID-EX-MEM-WB pipeline **with no bypassing**, for each segment of code, indicate the number of cycles it would take to completely execute:

a. ADD r1, r2, r3
   SUB r5, r4, r6
   LW r7, $300(0)
b. ADD r3, r2, r4
   SUB r5, r3, r7
   LW r1, $200(0)
c. LW r5, $100(0)
   ADD r4, r5, r7
   SUB r5, r1, r6

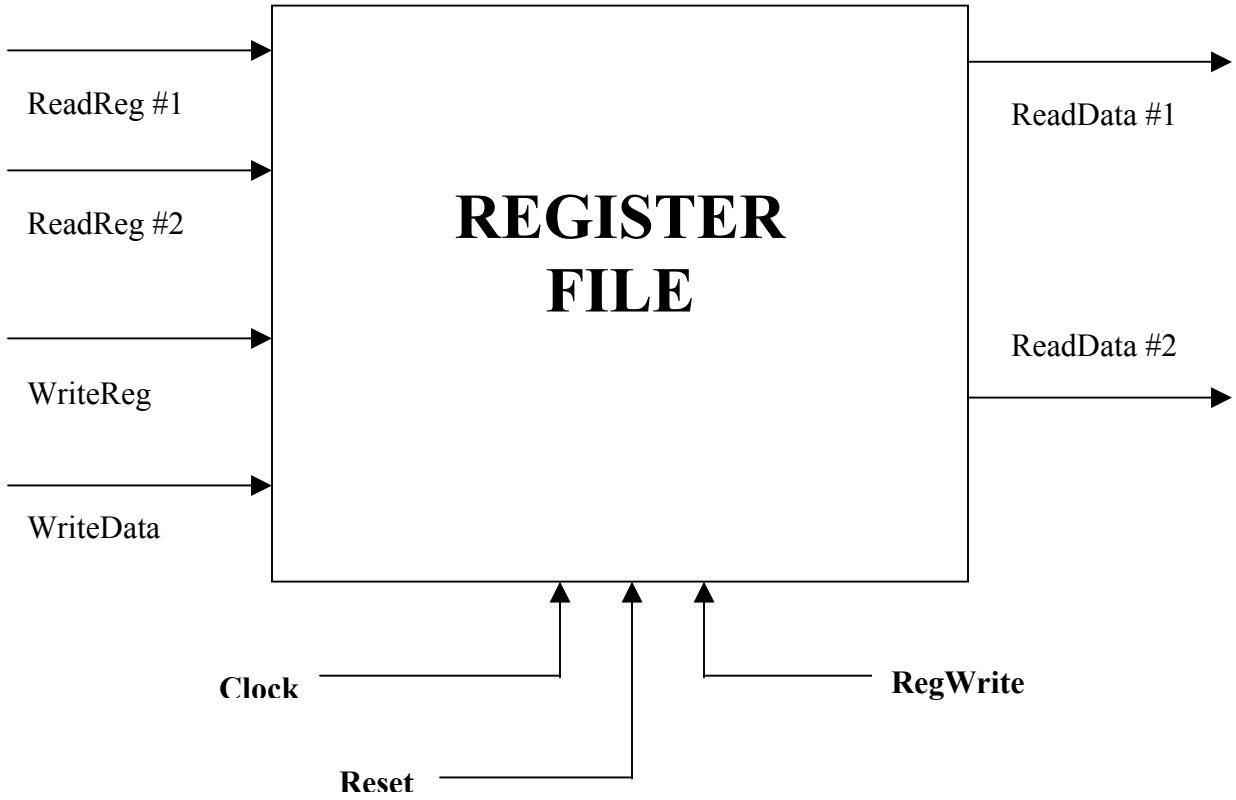
2. (15 points - 5 points each)
Using the standard IF-ID-EX-MEM-WB pipeline **with bypassing**, for each segment of code, indicate the number of cycles it would take to completely execute:

a. ADD r1, r2, r3
   SUB r5, r4, r6
   LW r7, $300(0)
b. ADD r3, r2, r4
   SUB r5, r3, r7
   LW r1, $200(0)
c. LW r5, $100(0)
   ADD r4, r5, r7
   SUB r5, r1, r6

3. **(35 points)** *Mentor Graphics Design and Simulation*
Using Mentor Graphics DA, design a Register-File of sixteen 16-bit registers. It has three 16-bit data buses **ReadReg1, ReadReg2** and **WriteData**, a write control signal **RegWrite** and **Clock, Reset** inputs. The data on ReadData1 and ReadData2 corresponds

to addresses on ReadReg1 and ReadReg2 respectively. The data on WriteData gets written into the register specified by WriteReg at the rising edge of the clock when the RegWrite signal is high. Furthermore, $0 always reads zero, irrespective of what is written to it and $15 is initialized to value xFFFE on reset. All other registers are reset to x0000 when **Reset** is low.

Each 1-bit Flip-flop has a delay of 6ns**. DO NOT** use clock gating. Design your decoders etc. (if needed) using gates.



You should turn in the following

1. Design Architect Schematics of Register File.
2. QuickSim II Force File used to test the Register file.
3. Test various read-write combinations to a particular register in the Reg. File and submit trace and list window outputs for 10 different cases.

4. (25 points) *Mentor Graphics Design and Simulation*

Using Mentor Graphics DA, design a 4-bit Shifter Register with Parallel Load. It has two control signals **load** and **shift,** one serial input (**Si)**, four data inputs (**D0…D3)**, four outputs (**Q0…Q3)** and a **clock**. When both shift and load are low; there is no change, when shift is low and load is high; d0 – d3 is loaded and when shift is high; data is shifted down (Si->Q0, Q0->Q1, Q1->Q2, etc.).

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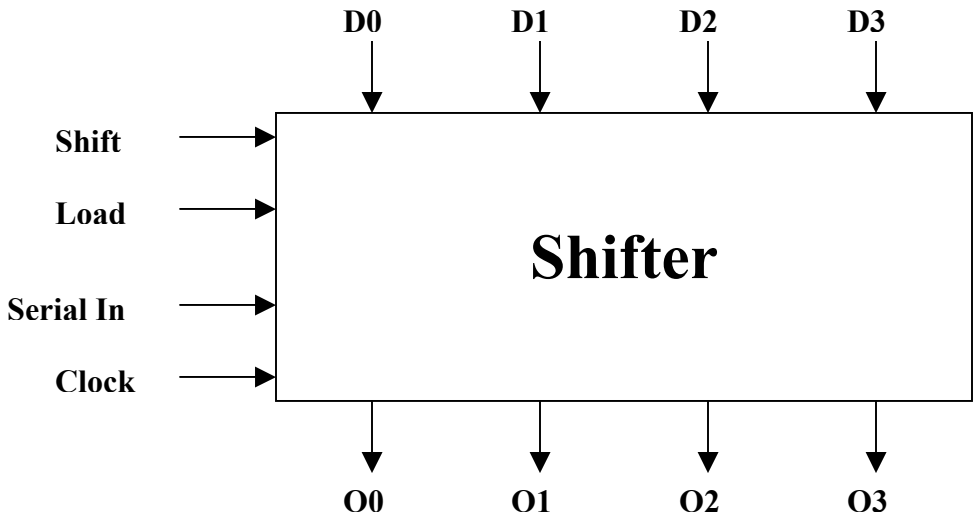

You should turn in the following

1. Design Architect Schematics of your Shifter.
2. QuickSim II Force File used to test your Shifter.
3. An output from the list window showing simulation results corresponding to your force file. **On one-page,** display enough of examples to show that your unit is functioning correctly.