

**ECE/CS 552: Introduction to Computer Architecture**  
**ASSIGNMENT #4**

**Due Date: In class November 16<sup>th</sup>, 2005**

This homework is to be done individually.

Total 4 Questions, 80 points

**1. (5 points) Cache Configurations**

Consider a system with a 2K-byte main memory, 256 byte **direct mapped** cache and line sizes of 16 bytes. How many lines are there?

**2. (15 points) Cache Configurations**

For the above cache, two 128-byte linear data arrays are going to be placed in the cache from main memory. If the first array starts at location 0 and the second array starts at location 320, how many of the cache lines result in conflicts when both arrays are accessed?

**3. (20 points - 15 for first, 5 for second) Cache Protocols**

Given a 2 Kbytes two-way set associative cache with 16 byte lines and the following code:

```
for (int i = 0; i < 1000; i++) {  
    A[i] = 40 * B[i];  
}
```

- Compute the overall missrate (assume array entries require one word)
- What kind of cache locality is being exploited?

**4. (40 points – 20 each) SimpleScalar Simulation**

This problem will introduce you to the SimpleScalar simulator (documentation is available from <http://www.simplescalar.com/>. Note that you will need a Unix account at CAE for this problem (all students in this class are eligible for accounts at CAE). The SimpleScalar 3.0 simulator is available at CAE in "`~ece552/simplesim-3.0`". You will use a script called "RUNgo" to run the go benchmark from the SPECint95 benchmark suite. Copy the files in "`~ece552/hw4`" to somewhere that you have write access.

a. "sim-cache" is a cache simulator in SimpleScalar. Report the L2 unified cache, L1 instruction cache, and L1 data cache miss rates, using the following command (run from your hw1 directory):

```
./RUNgo ~ece552/simplesim-3.0/sim-cache ./go.ss -cache:il1 il1:128:64:1:1 -cache:il2 dl2  
-cache:dl1 dl1:256:32:1:1 -cache:dl2 ul2:1024:64:2:1 >& outfile
```

This will run the go benchmark and simulate a two-level cache hierarchy with an 8K direct-mapped L1 instruction cache with 64 byte lines (128 sets, 64 byte lines, 1-way set associative, 'l' for LRU replacement policy), an 8K direct mapped L1 data cache with 32 byte lines (256 sets, 32 byte lines, 1-way set associative, 'l' for LRU replacement policy),

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and a 128K 2-way set associative unified L2 cache with 64 byte lines. The output of the simulation will be placed in "outfile".

b. Using the RUNgo script and the sim-cache tool, find the sizes of each of the three caches that will reduce the miss rates of each of the three caches by 50%. Report the configuration as well as the miss rate reported by sim-cache.