

ECE/CS 552: Introduction to Computer Architecture

Fall Semester 2005, MWF 2:25-3:15 EH2317

Instructor: Prof. Mikko Lipasti, mikko@engr.wisc.edu

TA: Daniel Chang, dwchang@wisc.edu

<http://www.cae.wisc.edu/~mikko/552/>

Course Description

This course provides an introduction to the design of uniprocessor computer systems. Material covered in this course includes instruction set design, addressing, datapath design, control path design and microprogramming, memory management, caches and memory hierarchies, and interrupts and I/O structures.

Prerequisites for the course are ECE/CS 352 and ECE/CS 354.

Course Textbook

D.A. Patterson and J.L. Hennessy, *Computer Architecture and Design: The Hardware/Software Interface*, 2nd edition, Morgan Kaufman Publishers. If you cannot find the (preferred) 2nd edition, buy the 3rd edition

Homework

There will be approximately 5 homework assignments which will not be weighted equally. Some assignments will require the review of material that is touched upon, but not covered in depth in class. Some homework assignments are to be completed individually, while for others you are expected to work in groups. No late homework will be accepted.

Project

The project is to implement a working non-pipelined processor that implements the WISC-F05 instruction set. Extra credit will be granted for a more aggressive pipelined implementation, but only if the baseline non-pipelined implementation also works correctly. The project is to be completed in groups of two or three students; no individual projects will be allowed. Successful completion of the project includes a demonstration and a written report that documents your design.

Mentor Graphics Tutorial

For both homework and project assignments you will rely heavily on the Mentor Graphics tools available in CAE. There will be two tutorial sessions for Mentor Graphics on 9/7 and 9/8 from 6-9pm, CAE175.

Examinations

There will be an in-class midterm examination and a comprehensive final on Friday, Dec 16, at 7:25pm.

Grading

Homework	20%
Midterm	30%
Final	30%
Project	20%

Communications Channels

I strongly encourage you to meet with me during my office hours, or call me or send e-mail. Introducing yourself to me, expressing concerns, offering suggestions, and seeking advice are among the welcome topics. Make

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sure you monitor the web site for this course which contains course information, lecture notes, pointers to project resources, and the latest announcements.

Office Hours

Prof. Lipasti: EH4613, M 10:00-11:00, R 1:00-2:00

TA: Daniel Chang, TBD

Course Outline

Week	Dates	Assignments	Topics	Readings
0	9/2		Introduction	Ch 1
1	9/7,9/9	HW1 out Mentor tutorial 9/7, 9/8	Performance and Cost	Ch 2
2	9/12,9/14,9/16		Instruction Sets	Ch 3
3	9/19,9/21,9/23	HW1 due, HW2 out	Arithmetic I	Ch 4.1 - 4.5
4	9/26,9/28,9/30		Datapath design	Ch 5.1 - 5.3
5	10/3,10/5,10/7	HW2 due, HW3 out	Control	Ch 5.4 - 5.9, App C
6	10/10,10/12,10/14	Project out	Pipelining	Ch 6.1 - 6.7
7	10/17,10/19,10/21	HW3 due	Intro to Superscalar	Ch 6.8 - 6.9
8	10/24,10/26,10/28		Review and Midterm 10/28	
9	10/31,11/2,11/4	HW4 out	Memory Technology	Ch 7.1, App B
10	11/7,11/9,11/11	HW4 due, HW5 out	Memory Hierarchies	Ch 7.2 - 7.6
11	11/14,11/16,11/18		Memory Hierarchies cont'd	Ch 7.2 - 7.6
12	11/21,11/23	HW5 due	Arithmetic II	Ch 4.6 - 4.10
13	11/28,11/30,12/2		I/O	Ch 8
14	12/5,12/7,12/9	Project report due 12/9 Project demos 12/11	Parallel processing	Ch 9
15	12/12,12/14		Review	--
16	12/16		Final Exam, 7:25pm Friday	--