
UNIVERSITY OF WISCONSIN

ECE 757 Adv. Computer Architecture II

Midterm Exam 1 - Ch. 1-5

Take-home exam, distributed October 17, 2000, Due back October 19, 2000

Name: _____

This exam is **open books, open notes, and open all handouts** (including previous homeworks and exams, project descriptions, textbook, and readings). **However, it must be your own work--do not discuss any aspects of the exam problems with other students until after the exams have all been turned in.**

Write all your answers in the space provided. If you use the back of any page, please clearly indicate on the front of the page.

If you feel there is ambiguity in the problem statement, please contact the TA or the professor. When in doubt, state your assumptions.

Problem 1. [45 points] _____ Cache Coherence

Problem 2. [25 points] _____ Shared Memory and Message Passing

Problem 3. [30 points] _____ Programming for Multiprocessor Systems

TOTAL: [100 points] _____

1. Cache Coherence [45 points]

Part A: State of cache using MSI [20 points]

You are trying to decide what cache coherence protocol to use for a two processor SMP system. The two processors are connected together using a simple electrically shared bus that does not perform split-transactions. You have taken a trace of the reads and writes of a parallel program on the system, with the reads and writes listed in the order in which they occur. In particular, you are looking at four different cache lines: A, B, C, and D. First look at two different types of MSI protocol. In the first version, which we call MSI1, a read to a line that is in the modified state in the other processor makes the line go from modified to shared. In the second version, called MSI2, the line goes from modified to invalid state. Specify the state of the cache lines after each read and write. Also specify the bus transaction that occurs for each read and write (the bus transactions are BusRead, BusReadX, BusUpgr, and BusWB).

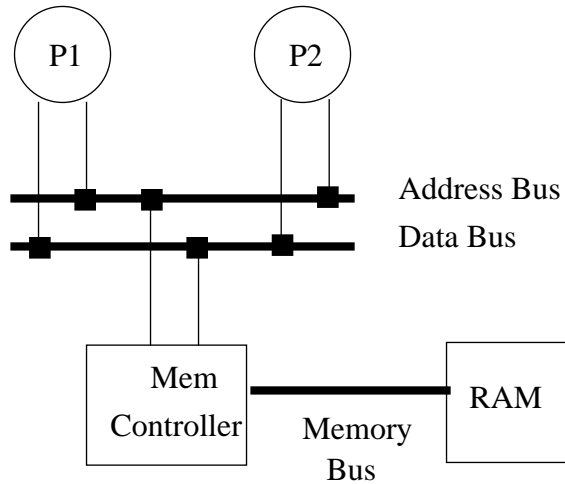
MSI1

Proc 1	Proc 2	A		B		C		D		Bus Transaction
										None
Read A										
	Write B									
Write C										
	Write D									
Write B										
	Read C									
Write A										
Read C										
Read D										
	Write D									

MSI2

Proc 1	Proc 2	A		B		C		D		Bus Transaction
										None
Read A										
	Write B									
Write C										
	Write D									
Write B										
	Read C									
Write A										
Read C										
Read D										
	Write D									

Part B: Improvements to MSI protocol [18 points]



For now, you have decided to use the first MSI protocol (MSI1). However, you would like to see if the MESI or MOESI protocols can improve the performance of the system. The above picture shows a diagram of the system. Specify how many transactions occur on each of the three buses (address bus, data bus, and memory bus) for the trace provided in Part A. Note that commands are sent across the address bus. Ignore all responses on the bus. (Remember to show all of your work)

Protocol	Address Bus	Data Bus	Memory Bus
MSI1			
MESI			
MOESI			

Part C: Designing an adaptive MSI protocol [7 points]

Rather than statically choose whether to go from the modified to shared or invalid state when the second processor performs a read of a line that is modified in the first processor's cache, you would like to use an adaptive method to choose which state to use. Propose a dynamic method for implementing this and justify your proposal by discussing the issues affecting your proposed design. Address the different types of sharing patterns that can occur and show how your mechanism will identify them effectively. Do not just optimize your mechanism for the trace used in part A, but take a step back and focus on the big picture.

2. Shared Memory and Message Passing [25 points]

[10 points] Explain why it is relatively easy to create a high performance implementation of message passing on shared memory, but difficult to create a high performance implementation of shared memory on top of message passing.

[15 points] Why would you want to use asynchronous message passing instead of synchronous message passing? Describe a scenario where asynchronous messages can be useful.

3. Programming for Multiprocessor Systems [30 points]

[12 points] Give an example of a program that works well with the following types of machines in Flynn's taxonomy: SIMD, MIMD, and SPMD. For each type, describe how the program would work and why the program would work better on that type of machine than on the other two types.

[10 points] In a cache coherent system that uses the MESI protocol, when a program uses a load-lock instruction for acquiring a lock, is it better to load the lock into the cache in exclusive or shared state. Why?

[8 points] In a shared memory system that implements Sequential Consistency, what are the legal outcomes of the code below? (Note that A, B, and C are initialized to 0)

P1

```
A = 4
if (B == 0)
    C = 1
```

P2

```
C = 2
if (B == 3)
    C = A
```

P3

```
if (A > 0)
    B = 3
```