

PERSONAL INFORMATION

Name: Dr. Michael J. Schulte
Date: April 21, 2008
Address: Dept. of ECE, University of Wisconsin-Madison
1415 Engineering Drive, Madison, WI 53706
Phone: (608)-262-0206
Email: schulte@engr.wisc.edu
Research Homepage: <http://mesa.ece.wisc.edu/>
Research Interests: Embedded processor architectures, computer architecture, computer arithmetic, digital system design, and domain-specific processing

EDUCATION

- Ph.D. in Electrical Engineering, University of Texas at Austin
Dissertation: *A Variable-Precision, Interval Arithmetic Processor*
Advisor: Earl E. Swartzlander, Jr.
Dissertation Committee: Harvey G. Cragon, Joydeep Ghosh, M. Ray Mercer, and Roy M. Jenevein
Area of Emphasis: Computer Engineering
Graduation Date: May, 1996
- M.S. in Electrical Engineering, University of Texas at Austin
Thesis: *Algorithms and Hardware Designs for Parallel Elementary Function Generation*
Advisor: Earl E. Swartzlander, Jr.
Second Reader: Harvey G. Cragon
Area of Emphasis: Computer Engineering
Graduation Date: December, 1992
- B.S. in Electrical Engineering, University of Wisconsin-Madison
Area of Emphasis: Computer Engineering
Second Major in Computer Science
Graduation Date: May, 1991

HONORS AND AWARDS

- International Conference on Computer Design Best Paper Award, 2007
- IBM Faculty Awards, 2004, 2006
- National Science Foundation CAREER Award, 1997-2001
- The Frank Hook Assistant Professorship - "Awarded to Lehigh's most outstanding junior scholar-teachers who also foster personal interaction and mentoring relationships with students," 2000. I was one of two Lehigh University faculty members to receive this award the first year it was offered.
- Lehigh University's Alfred Noble Robinson Award - "Recognizes outstanding performance in service to the university and unusual promise of professional achievement," 2000. Each year one or two Lehigh faculty members are selected to receive this award.
- IBM Faculty Partnership Award, 2000-2002
- IEEE Lehigh Valley Section Certificate of Appreciation, 2000
- Outstanding Faculty Advisor of the Year from Lehigh's National Society of Black Engineers, 1999-2000
- Faculty Award from Lehigh's National Society of Black Engineers, 1998-1999
- IEEE Best Counselor Award, Lehigh Valley Section, 1998
- IEEE Walter B. Morton Paper Contest, Supervised First Place Student Paper Award, 1998
- Outstanding Service Award from the Lehigh University S.T.A.R. Academy, 1998
- Certificate of Appreciation from Lehigh's National Society of Black Engineers, 1997-1998

- Reliable Computing, Best Student Paper Award, 1995
- TRW Graduate Fellowship, 1993-1996
- Microelectronic and Computer Development Fellowship, 1991-1993
- Basdall Garder MCD Fellowship, 1991-1993

ACEMEMIC EXPERIENCE

- Associate Professor with Tenure, Electrical and Computer Engineering, UW-Madison, 2006-present.
 - Performing and directing research in embedded and reconfigurable computing, computer architecture, design and evaluation of single-chip heterogeneous multiprocessors, processor architectures for software defined radio, computer clusters and graphics cards for 3D medical visualization and imaging, feedback systems for high-speed particle accelerators, and decimal floating-point arithmetic
 - Directing research supported by the National Science Foundation, the National Institutes of Health, Oak Ridge National Laboratories, IBM, Intel, and Sandbridge Technologies
 - Teaching the courses Digital Engineering Laboratory and Digital System Design and Synthesis
 - Leading a major update to the Digital Engineering Laboratory course including bringing in new computers, FPGA boards, and digital design software
- Assistant Professor, Electrical and Computer Engineering, UW-Madison, 2002-2006.
 - Performed and directed research in embedded processor architectures, reconfigurable computing, digital system design, computer architecture, computer arithmetic, and domain-specific processing
 - Researched and developed processor architectures, functional units, and software tools for domain-specific embedded processors
 - Founded and directed the Madison Embedded Systems and Architectures Laboratory
 - Taught various undergraduate and graduate courses including Advanced Topics in Embedded Systems, Embedded Computing Systems, Digital Engineering Laboratory, Digital System Design and Synthesis, Digital System Fundamentals, and Introduction to Microprocessor Systems
- Assistant Professor and Associate Professor with Tenure, Computer Engineering, Lehigh University, Bethlehem, PA, 1996-2002
 - Performed and directed research in computer architecture, computer arithmetic, embedded systems, application-specific processors, digital signal processors, and VLSI system design
 - Collaborated on joint projects related to domain-specific processor design and software tools with researchers from IBM, Sun Microsystems, Sandia National Laboratories, Lucent Technologies, Agere Systems, and Sandbridge Technologies
 - Founded and directed the Computer Architecture and Arithmetic Research Laboratory
 - Taught various undergraduate and graduate courses including Computer Architecture, Digital System Design, Advanced Computer Architecture, High-Speed Computer Arithmetic, and Application-Specific Processor Design
 - Established the National Society of Black Engineers Community Outreach Program and a National Science Foundation Summer Research Program for Minority Students
- Visiting Researcher, Sandia National Laboratories, Albuquerque, NM, Summer 1999
 - Researched and developed functional units for the Sandia Secure Microprocessor
 - Optimized the design and implementation of a Delta-Sigma A/D converter
- Research Assistant, University of Texas at Austin, Austin, TX, 1991-1996
 - Performed research in high-speed computer arithmetic and processor design
 - Researched and developed variable-precision interval arithmetic processors
- Grade School Teacher, St. Ignatius Martyr, Austin, TX, 1994-1995
 - Taught courses in mathematics, science, and English
 - Developed course curriculum and lesson plans

- Summer Research Assistant, Universität of Saarbrücken, Germany, Summer 1991
 - Developed routines in C++ for numerical computations
 - Reviewed research papers on systolic array architectures

INDUSTRY EXPERIENCE

- Technical Advisory Board Member, Sandbridge Technologies, White Plains, NY, 2005-2007
- Principal Consultant, Sandbridge Technologies, White Plains, NY, 2001-present
 - Assisted with the design and implementation of a multithreaded processor for software defined radio
 - Led the design of a multithreaded vector processing unit for the Sandbridge Sandblaster Processor
 - Wrote several patents dealing with architecture, microarchitecture, and hardware design features for software-defined radio
 - Investigated techniques for extending the Sandbridge Sandblaster Processor for multimedia, 3D graphics, and wireless security applications
 - Proposed and analyzed instruction set extensions for software defined radio
 - Investigated techniques for integrating reconfigurable hardware and low-power multithreaded processors
- Computer Architecture Consultant, AMD, Austin, TX, 2006-present
 - Investigated new architectures for high-performance, energy-efficient processors
 - Developed arithmetic algorithms and hardware designs for division and square root
 - Analyzed techniques for efficient initial approximations for reciprocal and reciprocal square root
 - Provided information and presentations on various computer arithmetic topics
- Computer Engineering Consultant, Coherent Logix, Austin, TX, 2006
 - Evaluated the architecture and microarchitecture of the Coherent Logix's HyperX Processing Element
 - Developed tools for testing floating-point instructions in the HyperX Processing Element
 - Developed algorithms and routines for reciprocal, square root, and reciprocal square root
- Expert Consultant, Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington, DC, 2007
 - Evaluated patents related to instruction set extensions, parallel operations, and multimedia processors
 - Examined prior art and claims charts dealing with multimedia processors and operations
- Expert Consultant, Atmel Corporation, San Jose, CA, 2006
 - Prepared an expert report related to the use of combined ASIC/FPGA systems
 - Evaluated patents related to ASICs and FPGA technology
- Expert Witness, Atmel Corporation, San Jose, CA, 2005
 - Prepared expert reports and provided testimony related to cell phone technology and embedded processors
 - Analyzed use of embedded processors in cellular telephones
- Computer Engineering Consultant, ARM Ltd., Austin, TX, 2003-2004
 - Analyzed approximation techniques for a 3D graphics processor
 - Provided feedback on techniques for high-speed reciprocal and reciprocal square root evaluation
- Computer Engineering Legal Consultant, Gateway, Inc., N. Sioux City, SD, 2004
 - Evaluated patents related to high-speed arithmetic circuits
- Computer Engineering Legal Consultant, Rambus, Inc. Los Altos, CA, Spring 2000
 - Reviewed patents on high-speed memory designs
 - Performed literature search on synchronous DRAM
- Compute Engineering Consultant, MIPS Technologies, Mountain View, CA, 1999
 - Developed techniques for high speed reciprocal and reciprocal square root computations

- Analyzed new algorithms for floating-point division and square root
- Computer Engineering Consultant, Cirrus Logic, Austin, TX, 1999
 - Developed Verilog models for a floating point adder/subtractor and comparator
 - Designed test benches for a floating point adder/subtractor
- Computer Engineering Consultant, Centaur Technology, Austin, TX, 1996
 - Developed algorithms and testing methodologies for transcendental functions
 - Designed and analyzed microcode routines for transcendental functions
- Computer Engineering Consultant, Analog Devices, Inc., Austin, TX, 1996
 - Performed error analysis for a systems of linear equations
 - Trained engineers to perform absolute and relative error analysis
- Intern Design Engineer, Crystal Semiconductor, Austin, TX, 1996
 - Modeled MPEG audio decoder in VHDL
 - Enhanced performance of a DSP chip
- Intern Design Engineer, Advanced Micro Devices, Austin, TX, 1994
 - Developed microcode algorithms for transcendental functions, division, and square root
 - Designed, implemented, and tested a multiple-precision microcode library
- Intern Design Engineer, Ross Technology, Austin, TX, 1993
 - Assisted in the design and development of an integer multiply and divide unit
 - Tested and debugged hardware for the HyperSparc microprocessor
- Engineering Co-op, McDonnell Douglas, St. Louis, MO, 1989-1990
 - Analyzed hardware and software implementations of neural networks
 - Assisted in designing an interface board for a satellite communication system

REFEREED JOURNAL ARTICLES

1. S. Mamidi, E. R. Blem, M. J. Schulte, J. Glossner, D. Iancu, A. Iancu, M. Moudgill, and S. Jinturkar, "Instruction Set Extensions for Software Defined Radio," accepted for publication in the *International Journal on Embedded Systems*, 2007.
2. L.-K. Wang and M. J. Schulte, "A Decimal Floating-Point Divider using Newton-Raphson Iteration," in the *Journal of VLSI Signal Processing Systems (Special Issue Featuring Extended Versions of Best Papers from ASAP2004)*, pp. 3-18, vol. 49, no. 1, October 2007.
3. S. Pieper, J. M. Paul, and M. J. Schulte, "A New Era of Performance Evaluation," in *IEEE Computer*, vol. 40, no. 9, pp. 23-30, September 2007.
4. J. Glossner, D. Iancu, M. Moudgill, G. Nacer, S. Jinturkar, S. Stanley, and M. Schulte, "The Sandbridge SB3011 Platform," in the *EURASIP Journal on Embedded Systems, Special Issue on Embedded Digital Signal Processing Systems*, vol. 2007, Article ID 56467, 16 pages, doi:10.1155/2007/56467, 2007.
5. P. Garcia, K. Compton, M. J. Schulte, E. Blem, and W. Fu, "An Overview of Reconfigurable Computing in Embedded Systems," in the *EURASIP Journal on Embedded Systems, Special Issue on Field-Programmable Gate Arrays in Embedded Systems*, vol. 2006, Article ID 56320, 19 pages, doi:10.1155/ES/2006/56320, 2006.
6. A. Akkas and M. J. Schulte, "Efficient Dual-Mode Floating-Point Multiplier Design and Implementation," in the *Journal of Systems Architecture*, vol. 52, no. 10, pp. 549-562, October 2006.
7. M. Gok, M. J. Schulte, and M. G. Arnold, "Integer Multiplier Designs with Overflow Detection," in *IEEE Transactions on Computers*, vol. 55, no. 8, pp. 1062-1066, August 2006.
8. M. J. Schulte, J. Glossner, S. Jinturkar, M. Moudgill, S. Mamidi, S. Vassiliadis, "A Low-Power Multithreaded Processor for Software Defined Radio," in the *Journal of VLSI Signal Processing (Special Issue Featuring Extended Versions of Best Papers from SAMOS2004)*, vol. 43, no. 2-3, pp. 143 – 159, June 2006.

9. K. E. Wires and M. J. Schulte, "Reciprocal and Reciprocal Square Root Units with Operand Modification and Multiplication," in *Journal of VLSI Signal Processing*, vol. 42, no. 3, pp. 257-272, March, 2006.
10. J. Liu, M.J. Redmond, E.K. Brodsky, A. Lu, F.J. Thornton, T.M. Grist, M. J. Schulte, J.G. Pipe, and W.F. Block, "Generation and Visualization of Four Dimensional MR Angiography Data Using an Under-sampled 3D Projection Trajectory," in *IEEE Transactions on Medical Imaging*, vol. 25, no. 2, pp. 148-157, February 2006.
11. R. D. Kenney and M. J. Schulte, "High-Speed Decimal Multioperand Adders," in *IEEE Transactions on Computers*, vol. 54, no. 8, pp. 953- 963, August 2005.
12. A. Akkas, J. E. Stine, and M. J. Schulte, "Inlining Interval Operations with Compiler Support," in *the Numerical Algorithms Journal (Special Issue Featuring Extended Versions of Best Papers from SCAN2002)*, vol. 37, pp. 13-20, December 2004.
13. M. J. Schulte, P. I. Balzola, A. Akkas, and R. W. Brocato, "Integer Multiplication with Overflow Detection or Saturation," in *IEEE Transactions on Computers – Special Issue on Computer Arithmetic*, vol. 49, pp. 681-691, July, 2000.
14. M. J. Schulte and E. E. Swartzlander, Jr., "A Family of Variable-Precision, Interval Arithmetic Processors," in *IEEE Transactions on Computers*, no. 5, vol. 49 pp. 387-398, May, 2000.
15. M. J. Schulte and James E. Stine, "Approximating Elementary Functions with Symmetric Bipartite Tables," in *IEEE Transactions on Computers*, no. 8, vol. 48, pp. 842-847, August, 1999.
16. J. E. Stine and M. J. Schulte, "The Symmetric Table Addition Method for Accurate Function Approximation," in *Journal of VLSI Signal Processing (Special Issue Featuring Extended Versions of Best Papers from ASAP97)* , vol. 21, no. 2, pp. 167-177, June, 1999.
17. M. J. Schulte, A. Akkas, V. Zelov, and J. C. Burley, "The Interval-Enhanced GNU Fortran Compiler," *Reliable Computing (Special Issue Featuring Extended Versions of Best Papers from SCAN1998)*, vol. 5., no. 3, pp. 311-322, 1999.
18. M. J. Schulte, K. C. Bickerstaff, and E. E. Swartzlander, Jr., "Hardware Interval Multipliers," *Journal of Theoretical and Applied Informatics*, vol. 3, no. 2, pp. 73-90, 1997.
19. T. Lynch and M. J. Schulte, "Software for High Radix On-line Arithmetic," *Reliable Computing*, vol. 2, no. 2, pp. 133-138, 1996.
20. M. J. Schulte and E. E. Swartzlander, Jr., "Variable-Precision, Interval Arithmetic Coprocessors," *Reliable Computing*, vol 2., no. 1, pp. 47-62, 1996.
21. T. Lynch and M. J. Schulte, "A High Radix On-line Arithmetic for Credible and Accurate Computing," *Journal of Universal Computer Science*, vol. 1, no. 7, pp. 435-449, 1995.
22. K. C. Bickerstaff, M. J. Schulte, and E. E. Swartzlander, Jr., "Parallel Reduced Area Multipliers," *Journal of VLSI Signal Processing (Special Issue Featuring Extended Versions of Best Papers from ASAP94)*, vol. 9, no. 3, pp. 181-192, April, 1995.
23. M. J. Schulte and E. E. Swartzlander, Jr., "A Software Interface and Hardware Design for Variable-Precision Interval Arithmetic," *Reliable Computing*, vol. 1, no. 3, pp. 324-342, 1995 (Best Student Paper Award).
24. M. J. Schulte and E. E. Swartzlander, Jr., "Hardware Designs for Exactly Rounded Elementary Functions," *IEEE Transactions on Computers – Special Issue on Computer Arithmetic*, vol. 43, no. 8, pp. 964-973, 1994.
25. M. J. Schulte, J. Omar, and E. E. Swartzlander, Jr., "Optimal Initial Approximations for the Newton-Raphson Division Algorithm," *Computing*, vol. 53, no. 3, pp. 233-242, 1994.
26. M. J. Schulte and E. E. Swartzlander, Jr., "Parallel Hardware Designs for Correctly Rounded Elementary Functions," *Interval Computations*, vol. 4, no. 4, pp. 65-88, 1993.

JOURNAL ARTICLES UNDER REVIEW

1. L.-K. Wang and M. J. Schulte, "Decimal Floating-Point Addition and Related Operations," submitted to the *IEEE Transactions on Computers*, July 2007.
2. M. Erle, M. J. Schulte, and B. J. Hickman, "Decimal Floating-Point Multiplication," submitted to the *IEEE*

Transactions on Computers, July 2007.

3. D. Tan, C. E. Lemonds, and M. J. Schulte, "Low-Power Multiple-Precision Iterative Floating-Point Multiplier with SIMD Support," submitted to the *IEEE Transactions on Computers*, July 2007.
4. C. Jenkins, S. Mamidi, M. J. Schulte, and J. Glossner, "Instruction Set Extensions for the Advanced Encryption Standard on a Multithreaded Software Defined Radio Platform," submitted to the *International Journal on Embedded Systems*, June 2007.
5. D. Iancu, H. Ye, J. Glossner, M. J. Schulte, S. Mamidi, and J. Takala, "Improved Spectral Efficiency through Iterative Concatenated Convolutional Reed-Solomon Software Decoding," submitted to the *IEEE Transactions on Communications*, September 2006.

JOURNAL GUEST EDITORIALS

1. M. J. Schulte, S. Bhattacharyya, and R. Schreiber, "Guest Editorial," *Special Issue of the Journal of VLSI Signal Processing on Application-Specific Systems, Architectures, and Processors*, vol. 40, pp. 5-6, May 2005.
2. M. J. Schulte and J.-C. Bajard, "Guest Editors Introduction: Special Issue on Computer Arithmetic," *IEEE Transactions on Computers*, vol. 54, pp. 241-242, no. 3, March 2005.
3. M. J. Schulte and G. A. Jullien, "Guest Editorial," *Special Issue of the Journal of VLSI Signal Processing on Application-Specific Systems, Architectures, and Processors*, vol. 31, no. 2, pp. 75-76, June 2002.

CONFERENCE PROCEEDINGS EDITED

1. J.-C. Bajard and M. J. Schulte (Editors), *Proceedings of the 16th IEEE Symposium on Computer Arithmetic*, IEEE Computer Society Press, June, 2003.
2. M. J. Schulte, S. Bhattacharyya, and R. Schreiber (Editors), *Proceedings of the 2002 IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, IEEE Computer Society Press, July, 2002.
3. E. E. Swartzlander Jr., G. A. Jullien, and M. J. Schulte (Editors), *Proceedings of the 2000 IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, IEEE Computer Society Press, July, 2000.

REFEREED CONFERENCE PAPERS

1. J. Glossner, D. Iancu, M. Moudgill, S. Jinturkar, G. Nacer, S. Stanley, A. Iancu, H. Ye, M. J. Schulte, M. Sima, T. Palenik, P. Farkas, and J. Takala, "Implementing Communications Systems on an SDR SoC," accepted for publication in the *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, Las Vegas, NV, April 2008.
2. L.-K. Wang, C. Tsen, M. J. Schulte, and D. Jhalani, "Benchmarks and Performance Analysis for Decimal Floating-Point Applications," in *Proceedings of the IEEE International Conference on Computer Design*, Lake Tahoe, CA, pp. 164-170, October 2007. (Best Paper Award)
3. C. Tsen, S. Gonzalez Navarro, and M. J. Schulte, "Hardware Design of a Binary Integer Decimal-based Floating-point Adder," in *Proceedings of the IEEE International Conference on Computer Design*, Lake Tahoe, CA, pp. 288-295, October 2007.
4. B. J. Hickmann, A. Krioukov, M. J. Schulte, and M. A. Erle, "A Parallel IEEE P754 Decimal Floating-Point Multiplier," in *Proceedings of the IEEE International Conference on Computer Design*, Lake Tahoe, CA, pp. 296-303, October 2007.
5. M. J. Schulte, D. Tan, and C. E. Lemonds, "Floating-Point Division Algorithms for an x86 Microprocessor with a Rectangular Multiplier," in *Proceedings of the IEEE International Conference on Computer Design*, Lake Tahoe, CA, pp. 304-310, October 2007.
6. M. Sima, M. Senthilvelan, D. Iancu, J. Glossner, M. Moudgill and M. J. Schulte, "Software Solutions for Converting a MIMO-OFDM Channel into Multiple SISO-OFDM Channels," *Proceedings of the IEEE International Conference on Wireless and Mobile Computing, Networking and Communications*, White Plains, NY, October 2007.

7. S. Mamidi, M. J. Schulte, D. Iancu, and J. Glossner, "Reconfigurable Multithreaded Processors for Programmable Communication Systems," in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, Montreal, pp. 320-327, July 2007.
8. C. Tsen, M. J. Schulte, and S. Gonzalez Navarro, "Hardware Design of a Binary Integer Decimal-based IEEE P754 Rounding Unit," in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, Montreal, pp. 115-121, July 2007.
9. J. Glossner, D. Iancu, M. Moudgill, M. Schulte, and S. Vassiliadis, "Trends in Low Power Handset Software Defined Radio," in *Proceedings of the 7th International Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation*, Lecture Notes in Computer Science, Vol. 4599, Samos, Greece, pp. 313-321, July, 2007.
10. L.-K. Wang and M. J. Schulte, "Decimal Floating-Point Adder and Multifunction Unit with Injection-Based Rounding," in *Proceedings of the IEEE International Symposium on Computer Arithmetic*, Montpellier, France, pp. 56-65, June 2007.
11. M. Erle, M. J. Schulte, and B. Hickman, "Decimal Floating-Point Multiplication Via Carry-Save Addition," in *Proceedings of the IEEE International Symposium on Computer Arithmetic*, Montpellier, France, pp. 46-55, June 2007.
12. S. Mamidi, E. R. Blem, M. J. Schulte, J. Glossner, D. Iancu, A. Iancu, M. Moudgill, and S. Jinturkar, "Instruction Set Extensions for Software Defined Radio on a Multithreaded Processor," in *Proceedings of the ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems*, San Jose, CA, pp. 266-273, September 2005.
13. J. Glossner, M. Moudgill, D. Iancu, G. Nacer, S. Jinturkar, S. Stanley, M. Samori, T. Raja, M. J. Schulte, and S. Vassiliadis, "Future Wireless Convergence Platforms," in *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware-Software Codesign and System Synthesis*, New York, pp. 7-12, September, 2005.
14. L.-K. Wang and M. J. Schulte, "Decimal Floating-Point Square Root Using Newton-Raphson Iteration," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, Samos, Greece, pp. 309-315, July 2005.
15. S. Mamidi, D. Iancu, A. Iancu, M. J. Schulte, and J. Glossner, "Instruction Set Extensions for Reed-Solomon Encoding and Decoding," in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, Samos, Greece, pp. 364-369, July 2005.
16. M. A. Erle, E. M. Schwarz, and M. J. Schulte, "Decimal Multiplication with Efficient Partial Product Generation," in *Proceedings of the IEEE International Symposium on Computer Arithmetic*, pp. 21-28, Cape Cod, MA, June 2005.
17. E. G. Walters and M. J. Schulte, "Efficient Function Approximation Using Truncated Multipliers and Squarers," in *Proceedings of the IEEE International Symposium on Computer Arithmetic*, pp. 232-239, Cape Cod, MA, June 2005.
18. J. E. Stine and M. J. Schulte, "A Combined Two's Complement and Floating-Point Comparator," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 89- 92, May 2005.
19. R. D. Kenney, M. J. Schulte, and M. A. Erle, "A High-Frequency Decimal Multiplier," in *Proceedings of the IEEE International Conference on Computer Design*, pp. 26-29, San Jose, CA, October 2004.
20. L.-K. Wang and M. J. Schulte, "Decimal Floating-Point Division Using Newton-Raphson Iteration," in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, pp. 84-95, Galveston, TX, September 2004.
21. M. J. Schulte, K. Chirca, J. Glossner, H. Wang, S. Mamidi, P. I. Balzola, and S. Vassiliadis, "A Low-Power Carry Skip Adder with Fast Saturation," in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, pp. 269-279, Galveston, TX, September 2004.
22. K. Chirca, M. Schulte, J. Glossner, S. Mamidi, and S. Vassiliadis, "A Static Low-Power, High-Performance 32-bit Carry Skip Adder," in *Proceedings of the 2004 Euromicro Symposium on Digital System Design*, pp. 615-619, Rennes, France, September, 2004.
23. J. Glossner, M. J. Schulte, M. Moudgill, S. Jinturkar, T. Raja, G. Nacer, and S. Vassiliadis, "Sandblaster

- Low-Power Multithreaded SDR Baseband Processor,” in *Proceedings of the Workshop on Application Specific Processors*, pp. 53-60, Stockholm, Sweden, August, 2004.
24. M. Gok, M. J. Schulte, and S. Krithivasan, “Designs for Subword-Parallel Multiplications and Dot Product Operations,” in *Proceedings of the Workshop on Application Specific Processors*, pp. 27-31, Stockholm, Sweden, August, 2004.
 25. S. Krithivasan, M. J. Schulte, and J. Glossner, “A Subword-Parallel Multiplication and Sum-of-Squares Unit,” in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 273-274, Lafayette, LA, February, 2004.
 26. R. D. Kenney and M. J. Schulte, “Multioperand Decimal Addition,” in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 251-253, Lafayette, LA, February, 2004.
 27. J. Thompson, N. Karra, and M. J. Schulte, “A 64-bit Decimal Floating-Point Adder,” *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 297-298, Lafayette, LA, February, 2004.
 28. A. Akkas and M. J. Schulte, “A Quadruple Precision and Dual Double Precision Floating-Point Multiplier,” in *Proceedings of the 2003 Euromicro Symposium on Digital System Design*, pp. 76-81, Antalya, Turkey, September, 2003.
 29. M. A. Erle and M. J. Schulte, “Decimal Multiplication Via Carry-Save Addition,” in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, The Hague, pp. 348-358, June, 2003.
 30. M. J. Schulte, L. P. Marquette, S. Krithivasan, E. G. Walters, and J. Glossner, “Combined Multiplication and Sum of Squares Units,” in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, The Hague, pp. 204-214, June, 2003. (One of three finalists for the best paper award).
 31. M. G. Arnold, J. E. Garcia, and M. J. Schulte, “The Interval Logarithmic Number System,” in *Proceedings of the 16th IEEE Symposium on Computer Arithmetic*, Santiago de Compostela, Spain, pp. 253-261, June 2003.
 32. J. E. Garcia and M. J. Schulte, “A Combined 16-Bit Binary and Dual Galois Field Multiplier,” in *Proceedings of the IEEE Workshop on Signal Processing Systems*, San Diego, California, pp. 63-68, October, 2002.
 33. P. I. Balzola, M. J. Schulte, J. Ruan, and J. Glossner, and E. Hokenek, “Design Alternatives for Parallel Saturating Multioperand Adders,” in *Proceedings of the IEEE International Conference on Computer Design*, Austin, TX, pp. 172-177, September, 2001.
 34. K. E. Wires, M. J. Schulte, and J. E. Stine, “Combined IEEE Compliant and Truncated Floating Point Multipliers for Reduced Power Dissipation,” in *Proceedings of the IEEE International Conference on Computer Design*, Austin, TX, pp. 497-500, September, 2001.
 35. K. E. Wires, M. J. Schulte, and D. McCarley, “FPGA Resource Reduction Through Truncated Multiplication” in *Proceedings of the 11th International Conference on Field Programmable Logic and Applications*, Belfast, Ireland, pp. 574-583, August, 2001.
 36. K. C. Bickerstaff, E. E. Swartzlander, Jr., and M. J. Schulte, “Analysis of Column Compression Multipliers,” in *Proceedings of the 15th IEEE Symposium on Computer Arithmetic*, Vail, Colorado, pp. 33-39, June 2001.
 37. M. J. Schulte, P. I. Balzola, J. Ruan, and J. Glossner, “Parallel Saturating Multioperand Adders,” in *Proceedings of the ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems*, San Jose, California, pp. 172-179, November, 2000.
 38. J. Hormigo, J. Villalba, and M. Schulte, “A Hardware Algorithm for Variable-Precision Logarithm,” in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, Boston, Massachusetts, pp. 215-224, July, 2000.
 39. A. Goldovsky, B. Patel, M. Schulte, R. Kolagotla, H. Srinivas, and G. Burns, “Design and Implementation of a 16 by 16 Low Power Two’s Complement Multiplier,” in *Proceedings of the 2000 IEEE International Symposium on Circuits and Systems*, Geneva, Switzerland, vol. 5, pp. 345-348, May, 2000.
 40. J. Hormigo, J. Villalba, and M. Schulte, “A Hardware Algorithm for Variable-Precision Division,” in

Proceedings of the 4th Conference on Real Numbers and Computers, pp. 104-112, Dagstuhl, Germany, April, 2000.

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4. M. Sima, D. Iancu, J. Glossner, M. J. Schulte and S. Mamidi, "Software Based Geometry Operations for 3D Computer Graphics," in *Proceedings of the SPIE International Symposium on Electronic Imaging: Multimedia on Mobile Devices*, San Jose, CA, vol. 6074, pp. 104-112, January 2006.
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COMMITTEE REVIEWED CONFERENCE AND WORKSHOP PAPERS

1. J. Glossner, M. Moudgill, D. Iancu, S. Jinturkar, G. Nacer, and M. J. Schulte, "The Sandblaster SBX 2.0 Architecture," accepted for publication in the *Proceedings of the Software Defined Radio Technical Conference*, November 2007.
2. C. Jenkins, S. Mamidi, M. J. Schulte, and J. Glossner, "Instruction Set Extensions for AES Processing on a Multithreaded Software Defined Radio Platform, accepted for publication in *Proceedings of the 41st Asilomar Conference on Signals, Systems, and Computers*, November 2007. (Third Place in the Student Paper Contest)
3. A. K. Polisetti, S. Assadi, C. Deibele, J. Patterson, R. C. McCrady, and M. J. Schulte "A Digital Ring Transverse Feedback Low-Level RF Control System," in *Proceedings of the 22nd Particle Accelerator Conference*, June 2007.
4. D. R. Janes, M. J. Schulte, E. K. Brodsky, and W. F. Block, "Low Latency Interventional MRI Visualization using a GPU Cluster," in *Proceedings of the Joint Annual Meeting of ISMRM-ESMRMB*, May, 2007.
5. D. R. Janes, M. J. Schulte, E. K. Brodsky, and W. F. Block, "Rapid Vascular Rendering Using 4D Cluster Visualization," in the *ISMRM Workshop on Real-Time MRI: Dynamic Interactive Imaging and its Applications*, Santa Monica, CA, February, 2006.
6. E. R. Blem, S. Mamidi, M. J. Schulte, J. Glossner, D. Iancu, M. Moudgill, and S. Jinturkar, "Instruction Set Extensions for Cyclic Redundancy Check on a Multithreaded Processor," in the *Workshop on Media and*

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8. M. A. Erle, M. J. Schulte, and J. G. Linebarger, "Potential Speedup with Decimal Floating-Point Hardware," in *Proceedings of the Thirty Sixth Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, IEEE Press, pp. 1073-1077, November, 2002.
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11. K. E. Wires, M. J. Schulte and J. E. Stine, "Variable-Correction Truncated Floating Point Multipliers," in *Proceedings of the Thirty Fourth Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, pp. 1344-1348, IEEE Press, November, 2000.
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9. M. J. Schulte and E. E. Swartzlander, Jr., "A Processor for Accurate, Self-Validating Computing," *Scientific Computing and Validated Numerics*, Akademie Verlag, pp. 25-31, 1996.
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PATENTS

1. Y. Ho, M. J. Schulte, and J. Kelly, "System and Method for Improving the Accuracy of Reciprocal Square Root Operations Performed by a Floating-Point Unit," US Patent No., June, 2005.

PATENT APPLICATIONS

1. M. J. Schulte, C. E. Lemonds, and D. Tan, "Division with Rectangular Multiplier Supporting Multiple Precisions and Operand Types," May 2007.
2. H. Ye, J. Glossner, M. Moudgill, M. Senthilvelan, and M. Schulte, "Software Implementation of MIMO-OFDM Wireless Communication Systems," September, 2006.
3. M. J. Schulte, J. Glossner, E. Hokenek, and P. I. Balzola, "Processor Having Parallel Vector Multiply and Reduce Operations with Sequential Semantics," Application No. 11/096,921, April, 2005.
4. E. Hokenek, M. Moudgill, M. J. Schulte, and J. Glossner, "Multithreaded Processor with Multiple Concurrent Pipelines per Thread," Application No. 11/096,917, April, 2005.
5. J. Glossner, E. Hokenek, M. Moudgill, and M. Schulte, "Processor Having Compound Instruction and Operation Formats," Application No. 11/096,767, April, 2005.
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11. M. J. Schulte, P. I. Balzola, E. Hokenek, and J. Glossner, "Processor Reduction Unit for Accumulation of Multiple Operands With or Without Saturation," Application No. 10/841,261, May, 2003.
12. Y. Ho, M. J. Schulte, and J. Kelly, "System and Method for Improving the Accuracy of Reciprocal Operations Performed by a Floating-Point Unit," Application No. 20020116431, January, 2002.

INVITED SEMINARS

1. M. J. Schulte "A Low-Power Multithreaded Processors for Wireless Communication Systems," presented at AMD Advanced Architecture and Technology Lab, October, 2007.

2. M. J. Schulte "A Low-Power Multithreaded Processors for Wireless Communication Systems," presented at Carnegie Mellon University, February, 2006.
3. M. J. Schulte "A Low-Power Multithreaded Processor for Wireless Communication Systems," presented at University of Wisconsin-Madison, November, 2004.
4. M. J. Schulte "A Low-Power Multithreaded Processor for Wireless Communication Systems," presented at Advanced Micro Devices, November, 2004.
5. J. Glossner and M. J. Schulte "The Sandbridge Multithreaded Communications Processor," presented at Delft University of Technology, June 2003.
6. M. J. Schulte "Architectures and Arithmetic Units for Embedded Digital Signal Processors Processing and Embedded Systems," presented at University of Wisconsin-Madison, April 2002.
7. M. J. Schulte "Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems," presented at the Pennsylvania Infrastructure Technology Alliance Symposium, Harrisburg, PA, October, 2000.
8. M. J. Schulte "Arithmetic Units for Digital Signal Processing and Multimedia Systems," presented at University of Southern California, Information Sciences Institute, July, 2000.
9. M. J. Schulte, "Architecture Enhancements and Arithmetic Units for Digital Signal Processing and Multimedia Systems," presented at Rice University, March, 2000.
10. M. J. Schulte, "Hardware and Software for Accurate and Reliable Numerical Computations," presented at the University of Texas, February, 2000.
11. M. J. Schulte, "Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems," presented at the Pennsylvania Infrastructure Technology Alliance Advisory Board Meeting, Carnegie Mellon University, Pittsburgh, Pennsylvania, December, 1999.
12. M. J. Schulte, "Arithmetic Algorithms and Hardware Designs for Digital Signal Processing," presented at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York, October, 1999.
13. M. J. Schulte, "Hardware Designs for Accurate and Reliable Numerical Computations," poster presented at the National Science Foundation CAREER PI Meeting, Washington, DC, January, 1999.
14. M. J. Schulte, "Arithmetic Units for Digital Signal Processing," presented at Sandia National Laboratories, Albuquerque, New Mexico, November, 1998.
15. M. J. Schulte, "Variable-Precision, Interval Arithmetic Processors", presented at Lehigh University, John Hopkins University, University of California at San Diego, Ohio State University, University of New York at Buffalo, University of Maryland at College Park, and the University of Virginia, 1996.
16. M. Schulte, "Hardware Designs and Arithmetic Algorithms for Variable-Precision, Interval Arithmetic Processors," presented at Queens University of Belfast and Delft University of Technology, September, 1995.

RESEARCH GRANTS AWARDED

1. Co-Principal Investigator (with Katherine Compton as PI) on "CRI:CRD Benchmark Suite for Embedded and Reconfigurable Computing Research," National Science Foundation, \$240,000, 2008-2011.
2. Principal Investigator on "An Adaptive Mixed-Signal Feedback Damper System for the Spallation Neutron Source," UT-Battelle, LLC, (for research with Oak Ridge National Laboratory), \$214,823, 2006-2009.
3. Principal Investigator on "FPGA Programming and Simulation," UT-Battelle, LLC, (for research with Oak Ridge National Laboratory), \$27,750, 2007-2008.
4. Co-Principal Investigator (with Katherine Compton as PI) on "CRI-SGER: Benchmark Suite for Embedded and Reconfigurable Computing Research," National Science Foundation, \$171,712, 2006-2008.
5. Principal Investigator, "Platform Support for IEEE 754r Decimal Floating-Point Arithmetic in the BID Format," Intel Corporation, 2006-2009, \$137,293 (\$87,960.00 awarded for first two years).
6. Principal Investigator on "IBM Faculty Award: Design Exploration for Decimal Floating-Point Arithmetic," IBM, \$20,000, 2006-unrestricted.
7. Principal Investigator on "Embedded Processor Architectures," Sandbridge Technologies, \$20,000, 2006-

unrestricted.

8. Co-Principal Investigator (with Walter Block as PI and Frank Korosec, Russel Paul, John Pauly, Scott Reeder, Alexei Samsonov, Orhan Unal, and Karl Vigen as Co-PIs) on “Real-time 3D MRI Technologies for Therapy and Diagnosis,” the National Institutes of Health, \$1,264,000, 2006-2011.
9. Principal Investigator on “Collaborative Research on Enabling Design Strategies for Single Chip Heterogeneous Multiprocessors,” \$217,694, 2005-2008. Subcontract from Virginia Tech on the NSF proposal, “Enabling Design Strategies for Single Chip Heterogeneous Multiprocessors,” (with JoAnn M. Paul as PI).
10. Principal Investigator on “Processor Support for Commercial Applications,” UW-Madison Graduate School, \$41,222, 2005-2006.
11. Principal Investigator on “Embedded Processor Architectures,” Sandbridge Technologies, \$40,000, 2003-unrestricted.
12. Principal Investigator on “IBM Faculty Award: Design Exploration for Decimal Floating-Point Arithmetic,” IBM, \$25,000, 2004-unrestricted.
13. Co-Principal Investigator (with W. Pottenger as PI and H. Moo-Young, H. Odi, and G. Blank as co-PIs) on “A Lehigh Valley Partnership to Enhance STEM Education through G4-12 Teaching Fellows,” the National Science Foundation, \$1,415,412, 2003-2006.
14. Principal Investigator on “CAREER: Hardware Support for Accurate and Reliable Numerical Computations,” National Science Foundation, \$220,000, 1997-2002.
15. Co-Principal Investigator (With Walter Block as PI) on “4D Cluster Visualization for Clinical Evaluation of Cinematic 3D Magnetic Resonance,” UW-Madison Graduate School, \$17,430, 2004-2005.
16. Principal Investigator (With Terry Boulton as Co-PI) on “Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems,” Pennsylvania Department of Community and Economic Development, \$60,000, 2001-2003.
17. Principal Investigator “Ultra Low Power DSP Hardware,” IBM, \$40,000, 2000-2002.
18. Principal Investigator (With Terry Boulton as co-PI) on “Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems,” Lucent Technologies, \$75,000, 2000-2001.
19. Principal Investigator (With Terry Boulton as Co-PI) on “Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems,” Pennsylvania Department of Community and Economic Development, \$39,600, 2000-2001.
20. Principal Investigator on “Mathematical Optimization and Design of VLSI Sub-components,” Sandia National Laboratories, \$31,896, 1999-2000.
21. Principal Investigator (With Terry Boulton as Co-PI) on “Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems,” Lucent Technologies, \$55,000, 1999-2000.
22. Principal Investigator (With Terry Boulton as Co-PI) on “Compilers, Architectures, and Tools for Digital Signal Processing and Embedded Systems,” Pennsylvania Department of Community and Economic Development, \$30,000, 1999-2000.
23. Principal Investigator on “Design and Optimization of VLSI Systems and Reconfigurable Hardware,” Sandia National Laboratories, \$25,000, 1999.
24. Principal Investigator on “Compilers and Architectures for Digital Signal Processing,” Lucent Technologies, \$37,000, 1997-1999.
25. Principal Investigator on “Compilers and Architectures for Digital Signal Processing,” Pennsylvania Department of Community and Economic Development, \$50,000, 1997-1999.
26. Principal Investigator on “Compiler Support for Interval Arithmetic,” Sun Microsystems Inc., \$49,240 and over \$150,000 in computing equipment, 1997-1999.
27. Principal Investigator on “Cellular Communication Support,” Anadigics Inc., \$25,324, 1997-1998.

EDUCATION GRANTS AND EQUIPMENT DONATIONS AWARDED

1. Principal Investigator (with Kewal Saluja and Mike Morrow as Co-PIs) on “DIN Instructional

- Lab/Technology Proposal: ECE554 Capstone Design Lab Upgrade,” \$28,000, 2007.
2. Principal Investigator on “Xilinx University Program Equipment Donation,” Xilinx Corporation, Equipment valued at \$14,141, 2007.
 3. Principal Investigator (with Mikko Lipasti as Co-PI) on “Software for Network Processor Simulation,” Agere Systems. Software valued at \$75,000, 2003.
 4. Co-Principal Investigator (with Michael Redmond as PI and Barton Miller and Yu Hen Hu as Co-PIs), on “Student Projects Testbed for Paradyn Performance Measurement and Parallel Rendering,” Hewlett-Packard, Equipment valued at \$106,000, 2003.
 5. Co-Principal Investigator (with C. DeMarco as PI) on “Equipment Grant Proposal,” Intel Corporation, Equipment valued at \$137,796, 2002.
 6. Principal Investigator on “Xilinx University Program Equipment Donation,” Xilinx Corporation, Equipment valued at \$244,295, 2002.
 7. Co-Project Investigator (with Terry Boulton as PI and several other Lehigh CSE Faculty as co-PIs) on “Laying the Foundations for Computer Science and Engineering Educational Expansion,” the Lucent Foundation, \$100,000, 2001-2002.
 8. Project Director (With Terry Boulton as Co-PI) on “Increasing the Number of Ph.D. Degrees Awarded to Minority Students in Electrical Engineering and Computer Science,” Alfred P. Sloan Foundation, \$16,200 for recruiting, plus \$17,300 per Sloan Scholar with up to six Sloan Scholars, 1998-2001.

GRADUATED DOCTORAL STUDENTS - DISSERTATION ADVISOR

1. Suman Mamidi, “Reconfigurable Multithreaded Processors for Programmable Communication Systems,” graduated from UW-Madison with a Ph.D. in May 2007, Senior Engineer in the DSP Architecture Team at Qualcomm.
2. Liang-Kai Wang, “Processor Support for Decimal Floating-Point Arithmetic,” graduated from UW-Madison with Ph.D. in August 2007, Senior Design Engineer at AMD.
3. Mustafa Gok, Dissertation: “Integer Multiplication and Squaring with Overflow Detection,” graduated from Lehigh University with a Ph.D. in January 2004, Assistant Professor at Cukurova University, Turkey.
4. Pablo Balzola, Dissertation: “Saturating Arithmetic for Digital Signal Processors,” graduated from Lehigh University with a Ph.D. in May 2003, DSP System Designer at Sandbridge Technologies.
5. Ahmet Akkas, Dissertation: “Instruction Set Enhancements for Reliable Computations,” graduated from Lehigh University with a Ph.D. in January 2002, Assistant Professor at Koc University, Turkey.
6. Kent Wires, Dissertation: “Arithmetic Units for Digital Signal Processing and Multimedia,” graduated from Lehigh University with a Ph.D. in January 2001, Member of Technical Staff at Agere Systems.
7. James Stine, Dissertation: “Design Issues For Accurate and Reliable Arithmetic,” graduated from Lehigh University with a Ph.D. in January 2001, Associate Professor at Oklahoma State University.

CURRENT DOCTORAL STUDENTS - DISSERTATION ADVISOR

1. Mark Erle, “Algorithms and Hardware Designs for Decimal Multiplication,” expected graduation date May, 2008.
2. George Walters, “Using Truncated Multipliers and Squarers in High Performance DSP Systems,” expected graduation date August, 2008.
3. Douglas Janes, “Advanced Multi-dimensional MRI Reconstruction and Visualization with GPUs,” expected graduation date August, 2008.
4. Murugappan Senthilvelan, “CORDIC for a Multithreaded DSP Instruction Set Processor,” expected graduation date December, 2008.
5. Samuel Tsen, “Decimal Floating-Point Solutions using the Binary-Integer Decimal Encoding,” expected graduation date May, 2009.
6. Zaipeng Xie, “Design and Analysis of a Mixed-Signal Feedback Damper System,” expected graduation date May, 2009.

7. Jake Adriaens, "Heterogeneous Chip Multiprocessors," expected graduation date May, 2009.
8. Daniel Chang, "Chip-Level Programming," expected graduation date May, 2009.

GRADUATED MASTER'S STUDENTS - THESIS OR PROJECT ADVISOR

1. Anil Poliseti, Project: "Design and Analysis of a Mixed-Signal Feedback Damper System for Controlling Electron-Proton Instabilities in Proton Storage Rings," graduated August 2007 from UW-Madison, Design Engineer with Qualcomm.
2. Eric Jackowski, Project: "Mobile Graphics Processors," graduated May, 2007 from UW-Madison, Design Engineer with ATI Technologies.
3. JeongAh Park, Project: "Floating-Point Units for 3D Graphics Applications," graduated December, 2005 from UW-Madison, Design Engineer, Qualcomm.
4. Inge Yuwono, Project: "Optimizing and Enhancing a 64-bit Decimal Floating-Point Adder," graduated August, 2005 from UW-Madison, Software Designer, Mandli Communications.
5. Parikshit Narkhede, Project, "4D Visualization Cluster," graduated May, 2005 from UW-Madison, Verification Engineer, ATI Technologies.
6. Shamik Valia, Project: "Floating Point Units for Wireless 3D Graphics," graduated December, 2004 from UW-Madison, Design Engineer, Qualcomm.
7. Arisandi Widjaja, Project: "Multithreaded Network Processors," graduation December, 2004 from UW-Madison, Design Engineer, Plexus.
8. Nick Lindberg, Project: "Performance Evaluation of Decimal Floating-Point Arithmetic," graduated December, 2004 from UW-Madison, Verification Engineer, IBM.
9. Shankar Krithivasan, Project: "A Subword-Parallel Multiplication and Sum-of-Squares Unit," graduated August 2004 from UW-Madison, Design Engineer with Qualcomm.
10. Shalin Shah, Project: "A Decimal Software Implementation of the Revised IEEE-754R Standard for Floating-Point Arithmetic," graduated August 2004 from UW-Madison, Verification Engineer, Montalvo Systems.
11. Mark Lodermeier, Project: "Sum of Absolute Differences Hardware Accelerator for Motion Estimation Applications," graduated August 2004 from UW-Madison, Design Engineer, Intel.
12. Robert Kenney, Project: "Decimal Multiplication and Multioperand Addition," graduated May 2004 from UW-Madison, Verification Engineer, IBM.
13. Yogesh Kulkarni, Project: "Multithreaded Network Processors," graduated May 2004 from UW-Madison, Design Engineer, NVIDIA.
14. David Leonard, Project: "Re-Implementation of 4D Cluster Visualization," graduated December, 2003 with M.S. from UW-Madison, Verification Engineer, ATI Technologies.
15. John Thompson, Project: "A 64-bit Decimal Floating-Point Adder," graduated December, 2003 with M.S. from UW-Madison, Verification Engineer, Cray.
16. Kim-Huei Low, Project: "An Efficient and Flexible Hardware Design for the Advanced Encryption Standard," graduated December, 2003 with M.S. from UW-Madison, ASIC Design Engineer, Qualcomm.
17. Nandini Karra, Project: "A 64-bit IEEE-754 Compliant Decimal Floating-Point Adder," graduated August, 2003 with M.S. from UW-Madison, Design Engineer, Intel.
18. Jason Schlessman, Thesis: "Approximation of the Sigmoid Function and its Derivative Using a Minimax Approach," graduated January, 2003 with M.S. from Lehigh University, pursuing Ph.D. degree at Princeton University.
19. George Walters, Thesis: "Automatic Generation of FIR Filters," graduated June, 2002 with M.S. from Lehigh University, pursuing Ph.D. degree at Lehigh.
20. Matthew Pillmeier, Thesis: "Implementation Alternatives for Barrel Shifters," graduated January, 2002 with M.S. from Lehigh University, Design Engineer at Unisys.
21. Navindra Yadav, Thesis: "Architectural Design Options for ATM Switches," graduated June 1999 with M.S. from Lehigh University, Design Engineer at Cisco Systems.

22. Alexander Goldovsky, Thesis: "A 1.0 Nanosecond 32-Bit Prefix Tree Adder in 0.25 Micron Static CMOS," graduated June 1999 with M.S. from Lehigh University, Design Engineer at Telgen.
23. Mustafa Gok, Thesis: "Integer Multiplication with Overflow Detection or Saturation," graduated June 1999 with M.S. from Lehigh University, Assistant Professor at Cukurova University, Turkey.
24. Larry Fenstermaker, Thesis: "Current Mode Sense Amplifiers Applied to Dual Port Register Files," graduated January 1998 with M.S. from Lehigh University, Member of Technical Staff at Agere Systems.
25. Gerald Williams, Thesis: "Processor Support for Interval Arithmetic," graduated May 1998 with M.S. from Lehigh University, Member of Technical Staff at Agere Systems.

CURRENT MASTER'S STUDENTS - THESIS OR PROJECT ADVISOR

1. Christopher Jenkins, "Instruction Set Extensions for the Advanced Encryption Standard on a Multithreaded Software Defined Radio," expected graduation date May 2008.
2. Brian Hickman "Parallel Decimal Floating-Point Multiplication," expected graduate date May 2008.

UNDERGRADUATE STUDENT RESEARCH SUPERVISION

1. Jie Liu, "Benchmarks for Embedded and Reconfigurable Computing," UW-Madison, 2007.
2. Michael Anderson, "Benchmarks for Embedded and Reconfigurable Computing," UW-Madison, 2007.
3. Paula Aguilera, "Coprocessors for Galois Field Arithmetic and Elliptic Curve Cryptography," UW-Madison, 2007.
4. Benjamin Kopp, "A Secure MPEG Decoder," UW-Madison, 2005.
5. Ohan Oda, Research Topic: "4D Cluster Visualization," UW-Madison, 2004-2005.
6. Anand Chhatpar, Research Topic: "4D Cluster Visualization," UW-Madison, 2003-2004.
7. Jason Schlessman, Research Topic: "Hybrid Squaring Units," Lehigh University, 2001-2002
8. Alexander Posada, Research Topic: "Combined Interval and Floating Point Hardware," Lehigh University, 2000.
9. Joseph Di Mattina, Research Topic: "Combined Interval and Floating Point Hardware," Lehigh University, 2000.
10. Louis Marquette, Research Topic: "Processor Design and Simulation Using VHDL", Lehigh University, 1998-2001.
11. Kwado Osafo-Mafo, Research Topic: "Hardware Support for Interval Arithmetic," Lehigh University, 1999.
12. Angel Periera, Research Topic: "Internet Tools for Interval Arithmetic", Lehigh University, 1999.
13. Edwin Alicea, Research Topic: "Internet Tools for Interval Arithmetic", Lehigh University, 1999.
14. James Nixon, Research Topic: "Internet Tools For Accurate Function Approximations," Lehigh University, 1998.

OTHER RESEARCH SUPERVISION

1. Ahmet Akkas, Research Topic: "Decimal Floating-Point Arithmetic," Honorary Fellow from Koc University, Turkey, worked under my supervision at UW-Madison during 2007, Assistant Professor at the Koc University, Turkey.
2. S. Gonzalez Navarro, Research Topic: "Decimal Floating-Point Arithmetic," Honorary Fellow from the University of Malaga, Spain, worked under my supervision at UW-Madison during 2006 and 2007, Assistant Professor at the University of Malaga, Spain.
3. J. Hormigo, Research Topic: "Variable-Precision, Interval Arithmetic Algorithms," Visiting Research Scientist from the University of Malaga, Spain, worked under my supervision at Lehigh University during 1998 and 1999 and at UW-Madison during 2007, Associate Professor at the University of Malaga, Spain.

COURSES TAUGHT

- Spring 2008, ECE353, Introduction to Microprocessor Systems, UW-Madison, 16 students
- Fall 2007, Digital Engineering Lab, UW-Madison, 10 students
- Spring 2007, ECE551, Digital System Design and Synthesis, UW-Madison, 34 students
- Fall 2006, ECE551, Digital System Design and Synthesis, UW-Madison, 32 students
- Fall 2006, ECE751, Embedded Computing Systems, UW-Madison, 24 students
- Spring 2006, ECE551, Digital System Design and Synthesis, UW-Madison, 43 students
- Spring 2006, ECE554, Digital Engineering Laboratory, UW-Madison, 27 students
- Fall 2005, ECE352, Digital System Fundamentals, UW-Madison, 80 students
- Spring 2005, ECE353, Introduction to Microprocessor Systems, UW-Madison, 40 students
- Fall 2004, ECE554, Digital Engineering Laboratory, UW-Madison, 24 students
- Spring 2004, ECE352, Digital System Fundamentals, UW-Madison, 45 students
- Fall 2003, ECE551, Digital System Design and Synthesis, UW-Madison, 66 students
- Spring 2003, ECE902, Advanced Topics in Embedded Systems, UW-Madison, 35 students
- Fall 2002, ECE551, Digital System Design and Synthesis, UW-Madison, 71 students
- Spring 2002, ECE201, Computer Architecture, Lehigh University, 96 students
- Fall 2001, ECE401, Advanced Computer Architecture, Lehigh University, 35 students
- Spring 2001, ECE201, Computer Architecture, Lehigh University, 110 students
- Fall 2000, ECE450, Application-Specific Processor Design, Lehigh University, 16 students
- Spring 2000, ECE401, Advanced Computer Architecture, Lehigh University, 27 students
- Fall 1999, ECE319, Digital Systems Design, Lehigh University, 56 students
- Fall 1999, ECE450, Advanced Digital Systems Design, Lehigh University, 16
- Spring 1999, ECE201, Computer Architecture, Lehigh University, 83 students
- Fall 1998, ECE495, High-Speed Computer Arithmetic, Lehigh University, 21 students
- Spring 1998, ECE201, Computer Architecture, Lehigh University, 73 students
- Fall 1997, ECE401, Advanced Computer Architecture, Lehigh University, 28 students
- Spring 1997, ECE201, Computer Architecture, Lehigh University, 71 students
- Fall 1996, ECE495, High-Speed Computer Arithmetic, Lehigh University, 2 students

EDITOR SERVICE

- Associate Editor for the IEEE Transactions on Computers, 2003-present.
- Associate Editor for the Journal of VLSI Signal Processing, 2002-present.
- Guest Editor for the Journal of VLSI Signal Processing, Special Issue on Application-Specific Systems, Architectures, and Processors, May, 2005.
- Guest Editor for the IEEE Transactions on Computers, Special Issue on Computer Arithmetic, March 2005.
- Guest Editor for the Journal of VLSI Signal Processing, Special Issue on Application-Specific Systems, Architectures, and Processors, June 2002.

CONFERENCE PROGRAM OR GENERAL CHAIR

- General Chair for the 19th IEEE International Symposium on Computer Arithmetic, 2009.
- General Chair for the 42nd Asilomar Conference on Signals, Systems, and Computers, 2008.
- Program Chair for the 37th Asilomar Conference on Signals, Systems, and Computers, 2003.
- Program Co-chair for the 16th IEEE International Symposium on Computer Arithmetic, 2003.
- General Chair for the 13th IEEE International Conference on Application-specific Systems, Architectures and Processors, 2002.

- Program Co-chair for the 12th IEEE International Conference on Application-specific Systems, Architectures and Processors, 2000.

CONFERENCE COMMITTEE MEMBER

- Steering Committee Member for the IEEE International Symposium on Computer Arithmetic, 2003-present.
- Steering Committee Member for the IEEE International Conference on Application-specific Systems, Architectures and Processors, 2002-present.
- Program Committee Member for the 40th Asilomar Conference on Signals, Systems, and Computers, 2006.
- Program Committee Member for the IEEE International Symposium on Computer Arithmetic, 1999-present.
- Program Committee Member for the Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2005-present.
- Program Committee Member for the Workshop on Application-Specific Processors, 2005-2006.
- Program Committee Member for the IEEE International Conference on Application-specific Systems, Architectures and Processors, 2000-2003.
- Program Committee Member for the IEEE International Symposium on Circuits and Systems, VLSI Systems Track, 2002.
- Program Committee Member for the 35th Asilomar Conference on Signals, Systems, and Computers, 2001.

CONFERENCE TECHNICAL AREA, SESSION, OR PUBLICATION CHAIR

- Publications Chair for the Workshop on Application-Specific Processors, 2007.
- Session Chair on Signal Processing Circuit at the IEEE International Conference on Computer Design, 2007.
- Technical Area Chair on Architecture and Implementation at the 40th Asilomar Conference on Signals, Systems, and Computers, 2006.
- Session Chair on Computer Arithmetic at the IEEE International Conference on Application-specific Systems, Architectures and Processors, 2004.
- Session Chair on Models, Methods, and Tools at the IEEE International Conference on Application-specific Systems, Architectures and Processors, 2003.
- Technical Area Chair on Implementation Techniques and Methods at the 35th Asilomar Conference on Signals, Systems, and Computers, 2001.
- Session Chair on Division and Square Root at the 15th IEEE International Symposium on Computer Arithmetic, 2001.
- Session Chair on Undergraduate Research at the IEEE Frontiers in Education Conference, 2000.
- Session Chair on Computer Arithmetic at the Asilomar Conference on Signals, Systems, and Computers, 1997, 1999, 2000.
- Session Chair at the International Symposium on Scientific Computing, Computer Arithmetic, and Validated Numerics, 1998.
- Session Chair at the International Workshop on Applications of Interval Computations, 1995.
- Session Chair at the IEEE International Conference on Computer Design, 1995.

REVIEWER ACTIVITIES

- National Science Foundation Graduate Fellowship Reviewer, 2006
- Alfred P. Sloan Foundation Proposal Reviewer, 2001
- National Science Foundation ENG Proposal Reviewer, 2001

- National Science Foundation CISE Proposal Reviewer, 1998, 1999, 2000
- Reviewer for the journals
 - IEEE Transactions on Computers
 - IEEE Transactions on Circuits and Systems II
 - IEEE Transactions on VLSI Systems
 - IEEE Transactions on Neural Networks
 - IEEE Signal Processing Letters
 - Journal of Microcomputer Systems Architecture
 - Journal of VLSI Signal Processing
 - EURASIP Journal on Embedded Systems
 - Reliable Computing
 - International Journal of Smart Engineering System Design
- Reviewer for the conferences
 - IEEE International Symposium on Computer Arithmetic.
 - IEEE International Conference on Application-specific Systems, Architectures and Processors
 - IEEE International Conference on Computer Design
 - IEEE International Conference on Circuits and Systems
 - IEEE/ASEE Frontiers in Education Conference
 - International Symposium on Scientific Computing, Computer Arithmetic, and Validated Numerics
 - International Symposium on Embedded Computer Systems: Architectures, Modeling, and Simulation
- Reviewer for the books
 - Koren, *Computer Arithmetic Algorithms*, Prentice Hall, 1993
 - H. Cragon, *Memory Systems and Pipelined Processors*, Jones and Barlette, 1996
 - B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, Oxford Press, 2000
 - M. Flynn and S. Oberman, *Advanced Computer Arithmetic Design*, John Wiley & Sons, 2001
 - M. Ercegovic and T. Lang, *Digital Arithmetic*, Morgan Kaufman Publishers, 2003.
- Senior Member of the IEEE and IEEE Computer Society

SERVICE AT UW-MADISON

- Computer Engineering Area Coordinator, 2007-present.
- Member of the Workload Committee, 2007-present.
- Member of the Graduate Advising, MS Exam, and AGS Evaluation Committee, 2007-present.
- Member of the Salary Committee, 2006-2007.
- Member of the Undergraduate Advising Committee, 2005-2007.
- Member of the Undergraduate Curriculum Planning Committee, 2003-2005.
- Member of the Graduate Curriculum and AGS Evaluation Committee, 2003-2004.
- Member of the Graduate Fellowship and Recruiting Committee, 2003-2005.
- Graduate Student Advising, 2002-present.
- Undergraduate Student Advising, 2004-present.
- Speaker at Graduate Student Open House, 2004.

SERVICE AT LEHIGH UNIVERSITY

- Director of the Computer Architecture and Arithmetic Research Laboratory, 1997-2002.
- Chair of the Computer Science and Engineering Faculty Search Committee, 2001-2002.

- Chair of the Computer Architecture Doctoral Qualifier, 1996-2002.
- Mentor to Junior Faculty on NSF CAREER Awards, 2001-2002.
- Member of the S.T.A.R. Academy Advisory Board, 2001-2002.
- Member of the Computer Engineering Steering Committee, 2001-2002.
- Member of the Computer Science and Engineering Chair Search Committee, 2001-2002.
- Member of the Industrial and Systems Engineering Search Committee, 2001-2002.
- Member of the Computer Science and Engineering Community Committee, 2001-2002.
- Member of Electrical Engineering and Computer Science Faculty Search Committees, 1998-2001.
- Member of the College of Engineering and Applied Sciences Dean Search Committee, 2000-2001.
- Member of the Advisory Council for Information Services, 2001-2002.
- Member of the Graduate Co-op Committee, 2000-2001.
- Member of the EECS Microprocessor Laboratory Committee, 1999.
- Member of the Circuits and Systems Doctoral Qualifier Committee, 1999.
- Faculty Secretary for the Electrical Engineering and Computer Science Department, 1997-1999.
- Faculty Advisor to the National Society of Black Engineers, 1997-2002.
- Faculty Advisor to the Institute of Electrical and Electronics Engineers, 1996-2002.
- Provided Students from Lehigh's S.T.A.R. Academy Opportunities for Summer Research, 1998-2001.
- Established and Directed Lehigh University's National Society of Black Engineers Community Outreach Program, 1998-2001.
- Helped Establish a Ph.D. Program in Computer Engineering, 2000-2002.