ECE/Comp. Sci. 352 – Digital System Fundamentals

Homework #2

Fall 2000

Homework 2 covers materials in sections 2.5-2.8, 3.1-3.8, supplement 1. You need NOT turn in the homework. However, you are strongly advised to work it out. Short solutions will be posted on course web home page shortly. We encourage you to work with your classmates as a group so that you can learn from each other.

Problems labeled with an (*) indicate that a solution is available in the Prentice Hall companion Website Gallery.

1. (essential prime implicants) Text book problem 2-19(b), 2-19(c)
2. (simplification) Text book problem 2-20 (a), (c)
3. (simplification) Text book problem 2-21 (a)
4. (simplification with don’t cares) Text book problem 2-25 (a), (b)
5. (simplification with NAND gate) Text book problem 2-27(a)
6. *(Implementation with NAND) Text book problem 2-28 (a), (b)
7. *(multilevel realization with NAND) Text book problem 2-29(b)
8. *(multilevel realization with NOR) Text book problem 2-30(a)


23. Addition of two numbers $X = X_4X_3X_2X_1$ and $Y = Y_4Y_3Y_2Y_1$ is performed using the carry lookahead technique.

(i) Write the equations for $P_i$ (propagate), $G_i$ (generate) and $S_i$ (sum).

(ii) Write the equations for $C_2$, $C_3$, $C_4$ and $C_5$ as functions of $G_i$, $P_i$ and $C_1$.

(iii) For $X = 1100$ and $Y = 0110$ and $C_1 = 0$, write the values of $P_i$, $G_i$, $C_i$ and $S_i$ (for $i = 1, 2, 3, 4$) and $C_5$.

(iv) Two 4-bit carry lookahead adders (CLA) are connected to build an 8 bit adder. The connection is such that the first 4-bit CLA gives outputs (least significant bit) $S_1$ to $S_4$ and the other CLA gives outputs $S_5$ to $S_8$ (most significant bit). The carry out $C_4$ of the first CLA is the carry in of the second CLA. Assume that all input bits and their complements are available. Also assume that each CLA is implemented using AND, OR gates only. How many gate delays are required to generate $S_1$ to $S_4$? How many gate delays are required to generate $S_5$ to $S_8$?