23. Addition of two numbers \( X = X_4X_3X_2X_1 \) and \( Y = Y_4Y_3Y_2Y_1 \) is performed using the carry lookahead technique.

(i) Write the equations for \( P_i \) (propagate), \( G_i \) (generate) and \( S_i \) (sum).

Answer: \( P_i = X_i \oplus Y_i \), for \( i = 1, 2, 3, 4 \); \( G_i = X_i \cdot Y_i \), for \( i = 1, 2, 3, 4 \)

(ii) Write the equations for \( C_2, C_3, C_4 \) and \( C_5 \) as functions of \( G_i, P_i \) and \( C_1 \).

Answer:

\begin{align*}
C_2 &= G_1 + P_1 C_1 \\
C_3 &= G_2 + P_2 G_1 + P_2 P_1 C_1 \\
C_4 &= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_1 \\
C_5 &= G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 C_1
\end{align*}

(iii) For \( X = 1100 \) and \( Y = 0110 \) and \( C_1 = 0 \), write the values of \( P_i, G_i, C_i \) and \( S_i \) (for \( i = 1, 2, 3, 4 \)) and \( C_5 \).

Answer:

\[
\begin{array}{cccccccccccc}
P_1 & P_2 & P_3 & P_4 & G_1 & G_2 & G_3 & G_4 & C_2 & C_3 & C_4 & C_5 & S_1 & S_2 & S_3 & S_4 \\
0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & 0 & 0
\end{array}
\]

(iv) Two 4-bit carry lookahead adders (CLA) are connected to build an 8 bit adder. The connection is such that the first 4-bit CLA gives outputs (least significant bit) \( S_1 \) to \( S_4 \) and the other CLA gives outputs \( S_5 \) to \( S_8 \) (most significant bit). The carry out \( C_4 \) of the first CLA is the carry in of the second CLA. Assume that all input bits and their complements are available. Also assume that each CLA is implemented using AND, OR gates only. How many gate delays are required to generate \( S_1 \) to \( S_4 \)? How many gate delays are required to generate \( S_5 \) to \( S_8 \)?

Answer:

Six gate delays to generate \( S_1 \) to \( S_4 \) and total twelve gate delays to generate \( S_5 \) to \( S_8 \).