Homework #3

Fall 2000

Homework 3 covers materials in sections 3.8-3.12, 3.14, 4.1-4.2 Problems labeled with an (*) are challenging problems. You need NOT turn in the homework. However, you are strongly advised to work it out. Short solutions will be posted on course web home page shortly. We encourage you to work with your classmates as a group so that you can learn from each other.

1. (1’s and 2’s complement) Text book problem 3-38.
2. (Unsigned number subtraction with 2’s complement) Text book problem 3-39(a),(c).
4. (Signed number subtraction) Text book problem 3-42 (b), (c).
5. (Parallel Adder) Text book problem 3-45(a), (c).
15. *(Latches) If NOR-pair and NAND-pair latches are so useful, how about the NAND-NOR latch shown? Under what combination(s) of input signals x and y will it set (Q = 1), reset, hold (remain unchanged), and Undefined?

![Diagram](image-url)
16. Addition of two numbers \( X = X_4X_3X_2X_1 \) and \( Y = Y_4Y_3Y_2Y_1 \) is performed using the carry lookahead technique.

(i) Write the equations for \( P_i \) (propagate), \( G_i \) (generate) and \( S_i \) (sum).

(ii) Write the equations for \( C_2, C_3, C_4 \) and \( C_5 \) as functions of \( G_i, P_i \) and \( C_i \).

(iii) For \( X = 1100 \) and \( Y = 0110 \) and \( C_1 = 0 \), write the values of \( P_i, G_i, C_i \) and \( S_i \) (for \( i = 1, 2, 3, 4 \) and \( C_5 \)).

(iv) Two 4-bit carry lookahead adders (CLA) are connected to build an 8 bit adder. The connection is such that the first 4-bit CLA gives outputs (least significant bit) \( S_1 \) to \( S_4 \) and the other CLA gives outputs \( S_5 \) to \( S_8 \) (most significant bit). The carry out \( C_4 \) of the first CLA is the carry in of the second CLA. Assume that all input bits and their complements are available. Also assume that each CLA is implemented using AND, OR gates only. How many gate delays are required to generate \( S_1 \) to \( S_4 \)? How many gate delays are required to generate \( S_5 \) to \( S_8 \)?

The following are Verilog related problems. The solutions can be found at the companion website and will not be provided in the homework solution page.

17. (Verilog) Text book problem 3-76.