1. (20 points) signed binary number, decimal subtraction

(a) (12 points)
The following are two binary addition/subtractions performed in an unknown signed binary number representation. For each of them, determine their possible format (or formats) and whether there is an overflow occurred. Mark your answer in each blank box in the table below.

<table>
<thead>
<tr>
<th></th>
<th>Sign-Magnitude</th>
<th>1s complement</th>
<th>2s complement</th>
<th>Overflow?</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) $10110 - 01011 = 01011$</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>(b) $11001 - 10010 = 10111$</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(c) $01011 + 10111 = 00011$</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(b) (8 points) decimal arithmetics
Perform subtraction of two unsigned decimal numbers by taking the 10’s complement of the subtrahend. Answer only will NOT receive any credit. Your answer should include (i) 10’s complement of the subtrahend; (ii) the addition of the the minuend and the 10’s complement of the subtrahend. If the result is negative, you also need to give the answer in the form of $-A$ where $A$ is the magnitude of the answer.

Answer: $748 - 1051 = 0748 + 10C(1051) = 0748 + 8949 = 9697$. Since the end carry is 0, the result is negative. Thus, the answer should be $-(10’s$ complement of $9697) = -303$.

2. (15 points)
The logic diagram of a combinational logic circuit is given below:

Express the corresponding Boolean function in product of Maxterm format:

Answer: $f(a, b, c, d) = \overline{a} + \overline{b} + \overline{c} + \overline{d} = \prod M(15)$.

3. (20 points) MUX

(a) (10 points)
Assume Boolean variables \( w, x, y \), and their complements are available as inputs. Implement \( g(w, x, y) \) using a 4-to-1 Multiplexer. The switch control inputs are: \( s_1 = w \), and \( s_0 = x \).

\[
g(w, x, y) = w \cdot y + \overline{x} \cdot y + \overline{w} \cdot x \cdot \overline{y}.
\]

(b) (10 points) Find the corresponding Boolean function \( g(x, y, z) \) of the following multiplexer circuit. Represent the result in product of Maxterm format.

Answer:

Answer: \( g(x, y, z) = \prod M(0, 4, 5) \).

4. (15 points) Find the corresponding Boolean function of the following logic circuit. Give the result in \textit{simplified} sum of product (SOP) standard format.

Answer: \( f(A, B, C, D) = D(A \cdot (BC)) + D(A \cdot (BC)) = \overline{A} \cdot \overline{B}D + \overline{A} \cdot \overline{C}D + ABCD \).

5. (15 points) Adder and Carry Look-ahead adder. This problem will be graded on answers only.

Two four-bit unsigned (integer) numbers \( A = A_3A_2A_1A_0 = 0101 \), and \( B = B_3B_2B_1B_0 = 0110 \) are to be added.

For the \( i-th \) bit, its carry-in is denoted by \( C_i \), carry-out is denoted by \( C_{i+1} \), generate function denoted by \( G_i \) and propagate function denoted by \( P_i \).

Suppose that the XOR gate is implemented such that it has a propagation delay of \( 1.5\mu \) second, and all other AND, OR, or INVERTER gates all have a gate propagation delay of
1\mu\text{ second}. (1 \mu\text{ second} = 10^{-6}\text{ seconds}). Assume \{A_i, B_i; i = 0, 1, 2, 3\} and \(C_0\) are available simultaneously at time \(t = 0\).

(a) (6 points) \(C_3 = 1\). \(P_2 = A_2 \oplus B_2 = 0\); \(G_1 = A_1 \cdot B_1 = 0\).

If the addition is performed by a \textit{ripple carry adder} where each adder is realized with a partial full adder (PFA) and the carry is evaluated using the formula \(C_{i+1} = G_i + P_i \cdot C_i\).

(b) (3 points) \(C_2\) will be available is at \(t = 5.5\mu\text{ seconds}\).

\textbf{Answer:} \(P_i, G_i\) will be evaluated at \(1.5\mu\text{ s}\). \(C_i\) then will take additional \(2\mu\text{ s}\). \(C_2\) will be another \(2\mu\text{ s}\). Thus, in total, it will take \(1.5 + 2 + 2 = 5.5\mu\text{ s}\).

Now suppose that a four-bit carry-look-ahead adder is to be used to carry out this addition. Answer the following questions:

(c) (3 points) At the earliest, \(P_3\) will be available at \(t = 1.5\mu\text{ s}\).

(d) (3 points) At the earliest, \(S_3\) will be available at \(t = 5\mu\text{ s}\).

\textbf{Answer:} \(S_3 = P_3 \oplus C_3\). Hence \(S_3\) will be available \(1.5\mu\text{ s}\) after \(P_3\) and \(C_3\) are available. But \(C_3\) will taken \(2\mu\text{ s}\) after all \(P_i\) and \(G_i\) are available. From (c), \(P_i\) and \(G_i\) will take up to \(1.5\mu\text{ s}\) to evaluate. Hence \(S_3\) will take \(1.5 + 2 + 1.5 = 5\mu\text{ s}\) to evaluate.

6. (15 points) \textit{Verilog}

Consider the following structure \textit{Verilog} description of a combinational circuit. Sketch the logic schematic diagram of this circuit. Label input, output signals each wire, and each logic gate.

```verilog
module comckt(A, B, C, D, X, Y);
  input A, B, C, D;
  output X, Y;

  wire n1, n2, n3, n4, n5;
  not
    g1(n1, D);
  and
    g2(n2, B, C),
    g6(X, n4, n5),
    g7(Y, n3, n5);
  or
    g5(n5, n1, n2);
  nor
    g3(n3, A, n1);
  nand
    g4(n4, n1, n3);
endmodule
```

\textbf{Answer:} Figure 3-52, p. 168, text book.