1. (15 points) *Synchronous sequential circuit analysis*

Below is a Moore model sequential circuit.

(a) (6 points) Derive the flip-flop input equations.

**Answer:** \[ D = \overline{B} + X, \ J = \overline{A} + X = [A \cdot X], \text{ and } K = \overline{A} \oplus X \]

(b) (9 points) Derive the next state equation \( A(t+1) \) and \( B(t+1) \) and express the results in simplified Sum of Product standard form.

**Answer:** Use the flip-flop characteristic table at the end of the exam, we have

\[ A(t+1) = \overline{D(t)} = \overline{B + X} = \overline{B} \cdot \overline{X} \]

Also, \( B(t+1) = BJ + BK = \overline{X} \overline{B} + \overline{X} \overline{B} + B(A \oplus X) \)

2. (20 points) *Synchronous sequential circuit synthesis, simulation*

Given the state diagram of a sequential circuit as follows:

(a) (10 points) The table below is a hand simulation of a sequential circuit. Complete this table.

<table>
<thead>
<tr>
<th>Clock Cycle, t:</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Present State:</td>
<td>11</td>
<td>10</td>
<td>10</td>
<td>00</td>
<td>01</td>
<td>00</td>
</tr>
<tr>
<td>Present Input x(t):</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Present Output z(t):</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
(b) (10 points) Derive the corresponding two-dimensional state table of this sequential circuit.

<table>
<thead>
<tr>
<th>PS</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x=0</td>
<td>x=1</td>
</tr>
<tr>
<td>00</td>
<td>00</td>
<td>01</td>
</tr>
<tr>
<td>01</td>
<td>00</td>
<td>11</td>
</tr>
<tr>
<td>10</td>
<td>00</td>
<td>10</td>
</tr>
<tr>
<td>11</td>
<td>00</td>
<td>10</td>
</tr>
</tbody>
</table>

3. (30 points) synthesis

Consider the state table of a Moore model circuit below:

<table>
<thead>
<tr>
<th>Present State</th>
<th>$y_1(t) y_2(t)$</th>
<th>$y_1(t+1) y_2(t+1)$</th>
<th>Output $z(t)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>10</td>
<td>11</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>00</td>
<td>01</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>00</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>01</td>
<td>1</td>
</tr>
</tbody>
</table>

(a) (10 points) Sketch the corresponding state diagram.

(b) (5 points) Find the output equation in minimal SOP (sum-of-product) standard format.

Answer: $z(t) = y_2(t)$

(c) (15 points) If $y_1$ is realized with a D-type flip-flop, and $y_2$ is realized with a JK flip-flop. Derive the flip-flop input equations for $D_1$, $J_2$, and $K_2$ in minimum sum-of-products standard form. This part of problem will be graded on answer only.

Answer: Rewrite the state table as follows:
After Boolean simplification, we have

\[ D_1 = \overline{x}y_1y_2 + \overline{x}\overline{y}_2 + \overline{y}_1\overline{y}_2 \]
\[ J_2 = x\overline{y}_1 \]
\[ K_2 = \overline{x} \]

4. (15 points) *Flip-flop timing*

Complete the following timing diagram by drawing the waveforms for the outputs \( Q_1 \), \( Q_2 \), and \( Q_3 \) of the following clocked latches and flip flops (note the symbols). Assume all latches and FFs have been cleared at the beginning. Ignore gate delays.

5. (10 points) *Sequential Circuit Synthesis*
A virus detection program is designed to scan a stream of binary bits looking for a particular virus signature 10X1 where X is either 0 or 1. Upon detection of such a pattern, it gives an output 1 during the following clock cycle. Thus, it is designed as a Moore model sequential machine. An example of the input output relations is listed below:

<table>
<thead>
<tr>
<th>t</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>...</th>
</tr>
</thead>
<tbody>
<tr>
<td>x(t)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>...</td>
</tr>
<tr>
<td>z(t)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>...</td>
</tr>
</tbody>
</table>

Derive a state diagram. Label the starting state as S, and the other states as A, B, C, etc. If your answer has more than 6 states, it may contain redundant states and some points may be taken off even the solution is functional. To assist you to verify that your answer is correct, you may want to label each state with their definitions, such as receiving first 1 etc. You must sketch your answer within this page (back not included). Answers not in this page will not be graded nor reconsidered.

**Answer:**

![State Diagram](image)

6. (10 points) Verilog HDL
module p6_2(CLK, RESET, X, Z);
  input CLK, RESET, X;
  output Z;
  reg [1:0] state, next_state;
  parameter A = 2'b00, B = 2'b01,
                  C = 2'b10, D = 2'b11
  reg Z;
  always @(posedge CLK or posedge RESET)
    begin
      if (RESET)
        state <= 'B;
      else
        state <= next_state;
    end
  always @(X or state)
    begin
      case (state)
        'A: next_state = X ? 'A : 'B;
        'B: next_state = X ? 'D : 'B;
        'C: next_state = X ? 'A : 'C;
        'D: next_state = X ? 'D : 'C;
      endcase
    end
  always @(state)
    begin
      case (state)
        'A: Z = 1;
        'B: Z = 0;
        'C: Z = 0;
        'D: Z = 0;
      endcase
    end
endmodule

Displayed in the left side is a Verilog description of a certain mystery circuit. Based on this listing, answer the following questions.

(a) (3 points) In Verilog HDL, the construct begins with always @(posedge CLK or RESET) is called a

(b) (2 points) In Verilog HDL, the symbol <= is known as

(c) (3 points) If the present state is 01, and the input at the current clock cycle is X = 1, what would be the next state?

   Answer: D or 11.

(d) (2 points) Continue from part 6c of this problem, what would be the output at the present clock cycle?

   Answer: 0.