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ECE/Comp. Sci. 352 – Digital System Fundamentals

QUIZ # 4 (Spring 2000)

CLOSED BOOK
Thursday, April 27, 2000, 7:15 – 8:30 PM

<table>
<thead>
<tr>
<th>PROBLEM</th>
<th>POINTS</th>
<th>SCORE</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>15</td>
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<td>2</td>
<td>10</td>
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<td>5</td>
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<tr>
<td>6</td>
<td>20</td>
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<tr>
<td>TOTAL</td>
<td>100</td>
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</tbody>
</table>
1. (15 points) *Counters*

Below is the symbol of a 4-bit binary counter with parallel load. When load = 1, the count operation will be suspended and new data at $D$ will be loaded. Additional *glue logic* gates are to be added to this counter so that it will count the following sequence:

$$\{0, 1, 2, 3, 4, 7, 8, 9, 10\}$$

$Q_3$ is the most significant bit, and $Q_0$ is the least significant bit.
2. (10 points) shift register

Below is a linear feedback shift register constructed using a four bit shift register with parallel load plus a XOR gate. Initially, Shift = 0 and Load = 1 during the first clock cycle to load the input 1000. Then Shift = 1 during the rest of operation so that the shift register shifts down in the direction from $Q_0$ to $Q_3$. Fill in the following table:

<table>
<thead>
<tr>
<th>t</th>
<th>Shift</th>
<th>Load</th>
<th>$Q_3$, $Q_2$, $Q_1$, $Q_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X X X X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
3. (15 points) Registers

The function table of a register with two-bit control $S_1S_0$ is given below. $A_i(t)$, and $B_i(t)$ are respectively the present output and input of the $i^{th}$ bit of the register,

<table>
<thead>
<tr>
<th>Mode Control</th>
<th>Register Operation</th>
<th>Micro-operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$ $S_0$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0</td>
<td>No change</td>
<td>$A_i(t + 1) = A_i(t)$</td>
</tr>
<tr>
<td>0 1</td>
<td>Bitwise complement</td>
<td>$A_i(t + 1) = \overline{A_i(t)}$</td>
</tr>
<tr>
<td>1 0</td>
<td>Bit-wise OR</td>
<td>$A_i(t + 1) = A_i(t) + B_i(t)$</td>
</tr>
<tr>
<td>1 1</td>
<td>Parallel load</td>
<td>$A_i(t + 1) = B_i(t)$</td>
</tr>
</tbody>
</table>

(a) (5 points) Assume this is a four-bit register, $B = 0110$, and that $A$ is initially unknown. What is stored in $A$ after the following sequence of values on $(S_1, S_0)$ at successive positive clock edges? (*this part has no partial credit*)

<table>
<thead>
<tr>
<th>$t$</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1S_0$</td>
<td>11</td>
<td>01</td>
<td>10</td>
<td>00</td>
<td>01</td>
<td>00</td>
</tr>
<tr>
<td>$A(t)$</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(b) (10 points) Implement a single cell for this register by interconnecting a positive edge-triggered D flip-flop, and **minimum** number of AND, OR, NOT gates. Derive the flipflop input equation in simplified SOP format.

**Answer:** The flipflop input equation $D_i(t) =$
4. (15 points) Random Access Memory

An array of RAM ICs are used to construct a 256K Byte-addressable memory system in which each word is a byte. Each RAM IC has the configuration of 64K by 4.

(a) (3 points) How many RAM ICs are needed?  \textbf{Answer:} 

(b) (4 points) How many address lines and how many data lines are there for the memory system?

\textbf{Answer:} There are \underline{______} address lines and \underline{______} data lines.

(c) (3 points) Within each 64K by 4 RAM IC, how many memory cells are there? Write your answer in terms of power of two.

\textbf{Answer:} There are \underline{______} memory cells.

Now consider a 16K by 1 RAM IC. The 16K by 1 is the logical configuration only. Physically, the RAM cells are organized in a square array and two decoders (column select and row select) are used instead of a single row select decoder. This \textit{coincident selection} method will save hardware needed to implement large decoder and make the RAM chip's shape closer to a square.

(d) (2 points) Suppose that the column select and row select decoders are of the same size, how many address lines are connected to each decoder?

\textbf{Answer:} Each decoder has \underline{______} address lines connected to it.

(e) (3 points) Suppose the address lines of the most significant \(k\) bits of the address are connected to the row select decoder, and the remaining address bits are connected to the column select decoder. Find the row and column numbers of the RAM cell in the square array that corresponds to the Hexadecimal address \(20A3\).

\textbf{Answer:} The corresponding RAM cell is at the \underline{______} \(^{th}\) row and the \underline{______} \(^{th}\) column.
5. (25 points) Micro-operations

Below are three register transfer operations:

\[ S : \ PR \leftarrow 0, S \leftarrow 0, F \leftarrow 1, D \leftarrow 0 \]
\[ F : \ F \leftarrow 0, \text{if } AR = 0 \text{ then } D \leftarrow 1 \text{ else } R \leftarrow 1 \]
\[ R : \ PR \leftarrow PR + BR, AR \leftarrow AR - 1, R \leftarrow 0, F \leftarrow 1 \]

They are to be implemented with one parallel adder, three four-bit registers, AR, BR, and PR, four D-types flip flops, D, R, S, and F. All sequential circuits are of the positive edge triggered type. The AR register is also a down-counter. Its output are connected to a combinational logic zero detector. When the outputs of AR equal to zero, \( Z = 1 \). Otherwise, \( Z = 0 \). The PR register also has a \( \text{Clr} \) control. When \( \text{Clr} = 1 \), the content of PR will be cleared \textit{synchronously}. We assume before operation starts, both AR and BR have been loaded with appropriate contents. The operation begins by setting \( S = 1 \). A block diagram of this implementation is shown below:

(a) (10 points) Assume \( BR = 0011 \), and \( AR = 0010 \), and \( PR = 1110 \) initially. Perform hand simulation by completing the following table:

<table>
<thead>
<tr>
<th>clock cycle</th>
<th>S</th>
<th>F</th>
<th>R</th>
<th>D</th>
<th>AR</th>
<th>PR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0010</td>
<td>1110</td>
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<tr>
<td>1</td>
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</table>
(b) (12 points) Derive simplified Boolean expressions in SOP format for the following control signals as Boolean functions of $D$, $R$, $S$, $F$, and $Z$.

\[ D_{in} = \quad \quad R_{in} = \quad \quad \]
\[ F_{in} = \quad \quad Dec = \quad \quad \]
\[ L_P = \quad \quad Clr = \quad \quad \]

(c) (3 points) Derive the zero detection function $Z$ as a Boolean function of the output of $AR$ register, denoted by $a_3$, $a_2$, $a_1$, and $a_0$ respectively.

\[ \text{Answer: } Z = \quad \quad \]
6. (20 points) Buses

The following is a set of register transfer operations to be executed.

\[
\begin{align*}
R0 & \leftarrow R1 \\
R1 & \leftarrow R2 \\
R2 & \leftarrow R3 \\
R3 & \leftarrow R2 \\
R4 & \leftarrow R3 \\
R5 & \leftarrow R1 \\
\end{align*}
\]

(a) (5 points) If all 6 register transfer operations are to be executed in one clock cycle, how many buses are required? Briefly explain why.

Answer: \[\text{[ ]} \]. Explanation: 

(b) (10 points) If there is only a single bus available, schedule the execution of these 6 register transfer operations to minimize the total number of clock cycles needed. You should need fewer than 8 clock cycles.
(c) (5 points) Below is a single three-state bus configuration connecting three registers $R_0$, $R_1$, and $R_2$. Suppose the following two register transfer operations are to be implemented within a single clock cycle:

$$R_1 \leftarrow R_2; \quad R_0 \leftarrow R_2$$

What the values of the following control signals should be?