Last (Family) Name: ________________________________
First (Given) Name: ________________________________
Student ID: ________________________________

Department of Electrical and Computer Engineering
University of Wisconsin - Madison

ECE/Comp Sci 352
Digital System Fundamentals
Solutions - Quiz # 3
April 5, 2001

Closed Book Examination
90 minutes

1) No calculators, hand-held or laptop computers, cellular phones or pagers allowed.
2) If a box is provided, the contents of the box will be graded as the final answer.
3) Show your work for consideration of partial credit.
4) If you write anything on the back of a page and want it considered in the grading you must write “See back of page (give page number)” on the problem page.
5) A removable sheet with Boolean identities and theorems on one side and Verilog operators on the other side is given at the end of the exam.

<table>
<thead>
<tr>
<th>Problem</th>
<th>Points</th>
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<tr>
<td>1</td>
<td>16</td>
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<td>2</td>
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<td>5</td>
<td>18</td>
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<td>6</td>
<td>13</td>
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<td>Total</td>
<td>100</td>
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</table>
1. (b) (16) A very simple circuit containing flip-flops and latches is given below. You are to sketch carefully the output signals that result from the applied input signals. Assume that the propagation times and setup times are much shorter than the intervals between changes in the inputs.

![Circuit Diagram]

CLK
A
B
A
S
X
Unknown
B
R
A
J
Y
CLK
C
B
K
B
D
Z
CLK
C
2. (a) (9) Find sum-of-products (SOP) equations for $A(t+1)$ and $B(t+1)$ for the given circuit.

![Circuit Diagram]

\[ D_A = \overline{X} \overline{Y} A + B X + \overline{B} Y \]

Use JK characteristic table or equation.

\[ J_B = A Y, \quad K_B = A + X \]

\[ Q_B(t+1) = J_B + K_B \]

\[ A(t+1) = \overline{X} \overline{Y} A + B X + \overline{B} Y \]

\[ B(t+1) = A Y \overline{B} + \overline{A} \overline{X} B \]

(b) (8) Fill in the state table given for the equations given for $E(t+1)$, $F(t+1)$, $Z_1$ and $Z_2$.

\[ E(t+1) = X_2 E + \overline{X}_1 F \]

\[ F(t+1) = X_1 \overline{E} F + X_2 E \overline{F} + \overline{X}_1 \overline{X}_2 F \]

\[ Z_1 = E \overline{F} \]

\[ Z_2 = X_2 E F + X_1 \overline{E} \overline{F} \]

Note the 00, 01, 11, 10 order used in the table for $E$, $F$ and $X_1$, $X_2$ to permit you to use K-map methods for entry of values.
3. (a) (2) Does the state table given below represent a Mealy model or a Moore model? 
Circle one:  Mealy  Moore

(b) (8) Find the state diagram from the given state table; use the state circles provided. 
Note the 00, 01, 11, 10 order used for A,B in the table.

<table>
<thead>
<tr>
<th>X</th>
<th>X</th>
<th>A(t)B(t)</th>
<th>A(t+1)B(t+1)</th>
<th>A(t+1)B(t+1)</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>A(t)B(t)</td>
<td>A(t+1)B(t+1)</td>
<td>A(t+1)B(t+1)</td>
<td>Z</td>
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</tbody>
</table>

(c) (9) For the state diagram given below, find the sequence of states and outputs that results from the applied input sequence.

Input: 0 0 1 0 1 0 1 1 1 1
State: 0 0 0 1 0 1 1 1 1 1
Output: 1 0 1 0 0 0 1 0
4. (a) (2) A 2-dimensional state table has 37 rows.

1) What is a minimum number of state variables required to encode the states? **6**

2) How many unused states will there be in the table? **27**

The following table is for parts b and c. Note the 00, 01, 11, 10 ordering for the values for X,Y and A,B. This is to make it easy for you to construct K-maps using the information given.

<table>
<thead>
<tr>
<th></th>
<th>X Y</th>
<th>X Y</th>
<th>X Y</th>
<th>X Y</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 0</td>
<td>0 1</td>
<td>1 1</td>
<td>1 0</td>
</tr>
<tr>
<td>A(t)B(t)</td>
<td>A(t+1)B(t+1)</td>
<td>A(t+1)B(t+1)</td>
<td>A(t+1)B(t+1)</td>
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<tr>
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<td>1 0</td>
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<td>0 1</td>
<td>0 0</td>
<td>1 1</td>
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</tbody>
</table>

(b) (7) For the state table given above (outputs are irrelevant, so not given), find a minimum sum-of-products (SOP) flip-flop input equation for a **T flip-flop** for state variable **A**.

\[ T_A = Y + X \overline{A} \overline{B} + X A B \]

(c) (8) For the state table given above, find a minimum sum-of-products (SOP) flip-flop input equation for a **J-K flip-flop** for state variable **B**.

\[ J_B = \overline{X} Y A + X Y \]

\[ K_B = X \overline{A} + X Y \]
5. (a) (5) Draw the circuit diagram corresponding to the given Verilog description.

```verilog
module prob3_5a (X, Y);
    input [3:0] X;
    output [1:0] Y;
    wire [3:0] N;

    not N1 (N[0], X[3]),
        N2 (Y[0], N[1]);
    and A1 (N[1], N[0], X[2]),
        A2 (N[2], X[1], X[0]);
    or O1 (Y[1], N[0], N[2]);
endmodule
```

(b) (6) Draw the state diagram corresponding to the given Verilog description.

```verilog
module prob3_5b (X, RESET, CLK, Z);
    input CLK, RESET, X;
    output Z;
    reg [1:0] state, next_state;
    reg Z;
    always @(posedge CLK or posedge RESET)
        begin
            if (RESET)
                state <= 2'b00;
            else
                state <= next_state;
        end
    always @(X or state)
        begin
            //Ignore the next statement.
            next_state <= 2'bxx; Z = 1'bx;
            case (state)
                2'b00: begin
                    Z = 1'b0;
                    if (X == 1)
                        next_state <= 2'b01;
                    else
                        next_state <= 2'b00;
                end
                2'b01: begin
                    Z = 1'b0;
                    if (X == 1)
                        next_state <= 2'b01;
                    else
                        next_state <= 2'b10;
                end
                2'b10: begin
                    if (X == 1)
                        begin
                            next_state <= 2'b00;
                            Z = 1'b1;
```
5. (b) (Continued)

```verilog
  end
  else
    begin
      next_state <= 2'b10;
      Z = 1'b0;
    end
  endcase
end
endmodule
```

(c) (7) Complete the following Verilog dataflow description which is to compute:

1) the majority function \( M \) of \( A, B, \) and \( C, \) and
2) a selection function \( Y \) between \( A \) and \( B \) with \( C \) as the selection input.

The majority function is 1 if two or more of \( A, B, \) and \( C \) have value 1; otherwise, it is 0.

The select function is to form \( Y = A \) if \( C = 0 \) and \( Y = B \) if \( C = 1. \)

```verilog
module prob3-5c (A, B, C, M, Y);

input A, B, C;
output M, Y;

assign M = A & B | A & C | B & C
assign Y = C ? B : A // also, ~C & A | C & B

endmodule
```
6. (a) (6) The state diagram for a sequence recognizer for the subsequence 1 1 1 0 0 is to be determined. The sequence is to be recognized by producing a 1 output on Z when the last 0 is applied to X regardless of where the subsequence occurs in an overall sequence. The “backbone” of this diagram given below. You are to complete the diagram by adding the five arcs labeled with input/output value pairs needed. No credit will be given for a solution with states added.

(b) (7) A state diagram is to be developed for a circuit that is to generate the following sequence of values on its two outputs Z₁, Z₂: 1 0, 1 1, 0 1, 1 1 whenever a 1 occurs on its input X. Once it starts to produce the sequence the circuit ignores further 1’s until the sequence is completed. Except during the sequence, the outputs are 0 0. No credit will be given for a solution with states added.