ECE 551 - Digital System Design & Synthesis
Exercise 1 – Sections 2, 3, and 7 of IEEE Std 1364-2001
Spring 2003

Write in the answer at A: for each of the following questions and bring to class on Thursday, January 30 whether complete or not for use in the discussion.

1. Study sections 2.1 - 2.6.1, 2.7 - 2.7.4 of IEEE Std 1364-2001.

   Comments
   a. Write the word Verilog using the two forms for specifying comments:
      A:
      
   Constants
   b. Write x11010011 in hexadecimal as a constant of size 12.
      A:
   c. Write ’b x11010011 in hexadecimal as a constant of size 12.
      A:
   d. Write - 16’hFFF in binary.
      A:
   e. What is the decimal value of 8’hf?
      A:
   f. Write the following using sized hexadecimal with the hexadecimal digits grouped in threes beginning at the right using _: 00010010001101000110100010011010.
      A:

   Strings
   g. What in the size of the reg in bits required to store the string “Jane Doe”?
      A:

   Identifiers
   h. What are the only characters that can be used in a simple identifier other than letters and digits?
      A:
   i. Is an identifier of length 1025 characters allowable?
      A:

   Keywords, System Tasks and Functions
   j. All keywords must be lower case.
      A: True False
   k. Is the following in proper system function or system tasks format: $ stop
      A:

   Compiler Directives
   l. Where is the key located on a keyboard that you use for the open quote or accent grave used to begin a compiler directive?
      A:

**Logic Values**

a. Give the four basic Verilog signal values and their meanings
   A:
   A:
   A:
   A:

b. For normal logic gates, a z on a gate input is interpreted the same as an x.
   A: True False

c. Can all of these values appear in non-faulty hardware? Explain your answer.
   A:

**Nets and Variables**

d. Can a net store a value?
   A:

e. Can a variable store a value?
   A:

f. What are the variable datatypes?
   A:

g. What is the default initial value for variable datatypes?
   A:

h. Give the scalar or vector declarations for each of the following:
   1) Two vector registers, A and B, with bits numbering 7 to 0 from MSB to LSB.
      A:
   2) Three scalar wires, enable, RESET, and run.
      A:
   3) A wire mixed with bits numbered from –4 to 10. How many bits are there in mixed?
      A:
   4) A designated three-state bus tbus with bit numbering 0 to 15 from MSB to LSB
      A:

i. A variable is declared as follows. reg vectored [31:0] data_out; data_out is referenced later in an expression as data_out[15:0]. Is this permitted? Explain.
   A:

j. Circle the net type(s) can have multiple drivers:
   A: tri wire wand

k. What assignment type can be used to assign a value to a reg type?
   A:

l. A variable of the integer type can be used for declaring a hardware register?
   A: True False

m. A variable of the time type is used for simulation time quantities?
   A: True False
Arrays

n. Write declarations for the following arrays:
   1) A reg type array `regfile` with 32 8-bit registers.
      A:
   2) A memory SRAM with 32 bit data size and a 14-bit address size
      A:

Parameters

o. A parameter is a constant.
   A: TRUE FALSE

p. Declare the codes for the states of a sequential circuit as a single parameter declaration
   based on the following table:

<table>
<thead>
<tr>
<th>State Name</th>
<th>State code</th>
</tr>
</thead>
<tbody>
<tr>
<td>idle</td>
<td>00</td>
</tr>
<tr>
<td>brew</td>
<td>01</td>
</tr>
<tr>
<td>warm</td>
<td>10</td>
</tr>
<tr>
<td>unused</td>
<td>11</td>
</tr>
</tbody>
</table>

A:


   a. Specify in a single statement three instances of NAND gate with the following instance
      names and inputs and outputs:
         1. g1 inputs: x1, x2 output n1
         2. g2 inputs: x1, x3 output n2
         3 g3 inputs: n1, n2 output z0
      A:
   b. What is the control value for which a `bufif1` has a z output?
      A:
   c. Specify a not gate with input x1 and output x2 with a delay of 5 time units.
      A:
   d. Specify a not gate with input x1 and output x2 with a rising delay of 4 time units
      and a falling delay of 2 time units.
      A:
   e. Specify a bufif1 gate with input x1 and output x2 with a rising delay of 6 time units,
      a falling delay of 3 time units, and a turn-off delay of 4 time units.
      A:
   f. Specify a NOR gate with inputs x1 and x2 and output z0 with 1) a rising delay of 6
      time units max, 5 time units typical and 4 time units minimum, and a falling delay of 3
      time units maximum, 2.5 units typical, and 2 units minimum.
      A: