Department of Electrical and Computer Engineering
University of Wisconsin-Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2014-2015

Instructors: Kewal K. Saluja, 4611 Engr. Hall
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Credits: 3

Prerequisite: ECE/CS 352, Comp. Sci. 367;
ECE 353 or 552 or Consent of instructor

Goals: To be able to generate test vectors for complex digital (combinational and sequential) circuits; to understand and develop algorithms for automatic test pattern generation; and to be able to design circuits so that they are easy to test or can test themselves.

Topics: Test Economics
Fault Modeling and Fault Simulation
Test Generation Algorithms
Functional testing including Memory testing
Design for Testability including boundary scan
Built-In Self-Test
Test Techniques (such as Iddq testing)
Analog testing (time permitting)


Computer Usage: A project will be assigned during the semester which will require test generation, fault simulation, and fault diagnosis for a virtual chip using CAD software on CAE computing platforms. Limited number of projects that will entail development of ATPG related tools may also be assigned.

Grading Policy: 20% Homeworks
(tentative) 20-25% Project
25% Midterm Exam
30-35% Final Exam