WARNING: Go over all instructions before beginning your work.

There are two distinct parts to this document. First is Phase 4 which is the completion of the comparator design and its evaluation. Although specific instructions are given for Phase 4, there is no reporting associated with it. Anything that would ordinarily be reported in Phase 4 will be associated with the Final Report which is specified in the second part of this document.

Duties are to be shared equitably among team members; each team member is to review the work of the other for correctness and design quality to insure good results. This review which is to be done in detail has two goals: 1) to improve the quality of the project and 2) to make sure that both team members are familiar with all aspects of the material the project covers.

SPECIFICATIONS

The following specifications apply to all logic gates including inverters and flip-flops. 

**HSPICE model:** ~kime/public_html/spice_models/scn06hp.L13

- $V_{DD} = 3.3 \, V$
- $V_{OH} \geq 3.2 \, V$
- $V_{OL} \leq 0.1 \, V$
- $V_{th} = 1.65 \pm 0.55 \, V$
- $NM_H$ and $NM_L \geq 0.7 \, V$
- $\lambda = 0.3 \, \mu, \, \lambda/2 = 0.15 \, \mu$
LAYOUT SPECIFICATIONS

\[ L_{\text{drawn,min}} = 0.6 \, \mu \text{m} \quad \text{and} \quad W_{\text{drawn,min}} = 0.9 \, \mu \text{m} \]

\[ \Delta L_n = 0.14 \, \mu \text{m} \quad \text{and} \quad \Delta W_n = 0.50 \, \mu \text{m} \quad \text{(for manual calculations)} \]

\[ \Delta L_p = 0.21 \, \mu \text{m} \quad \text{and} \quad \Delta W_p = 0.53 \, \mu \text{m} \quad \text{(for manual calculations)} \]

\[ C_{\text{int, internal,max}} = 30 \, \text{fF} \quad \text{(represents a long local interconnect)} \]

\[ C_{\text{output,max}} = 500 \, \text{fF} \quad \text{(represents a moderately long global interconnect including FO loading)} \]

\[ f_{\text{minimum}} = 100 \, \text{MHz} \]

\[ f_{\text{typical}} = 120 \, \text{MHz} \]

\[ P_{\text{total}} \quad \text{(evaluated at 120MHz)} = \text{minimum} \]

\[ A \quad \text{(bounding box area)} = \text{minimum} \quad \text{(bounding box -- a box just large enough to contain the entire cell)} \]

\[ t_{\text{PHL}} \quad \text{-- as determined in your phase 1 (with specified multiple for the flip-flop)} \]

\[ t_{\text{PLH}} \quad \text{-- as determined in your phase 1 (with specified multiple for the flip-flop)} \]

\[ \text{FO} \quad \text{-- as determined in your phase 1} \]

LAYOUT SPECIFICATIONS

The layout style is to be a polycell (stacked standard cell) style in which there are rows of logic gates with spaces between rows for routing interconnections between gates. These spaces are called routing channels. The general structure of the layout is shown below. You will be designing and laying out the standard cells and then, from a modified version of your logic diagram done in da, will use automatic place and route to produce your comparator design.

A typical gate cell should take the form of Figures 7.14 and 7.15 in the text. The Metal VDD and GND “rails” are 10 \( \lambda \) wide and have their center lines spaced 80 \( \lambda \) apart for our technology. Metal 1 will be used for most, if not all, horizontal connections in the routing channels. It can be used in either direction within the cells. Metal 2 will be used for most,
if not all, vertical connections. Metal 2 should not be used within the standard cells except as ports. Cells should be designed so that they can be butted against adjacent cells of any kind on the left and the right without design rule violations. There is to be one substrate contact per each pair of nFETs and one well contact for each pair of pFETs. All signal inputs and outputs should be near the vertical center of the cell and all ports to connect to the cell should be Metal 2. Ports should be located so that all of them can be simultaneously reached by Metal 2 interconnect from the top and bottom of the cells.

The layers used for the interconnections between the standard cells should be Metal 1 and Metal 2. Inputs and outputs may lie anywhere around the edges of the layout, but may not be in its interior.

### PHASE 4

In this final phase, you are to do 1) the final design, 2) layout, and 3) simulations of your interval timer. In your design, you need not include flip-flops on the inputs except for those inputs which are the origin of critical paths. If there are many critical paths, then flip-flops need to be included only on up to five such paths.

#### Buffering

Anywhere that internal buffering is required, use “trees” of inverters as needed. The true and complement outputs of the two output flip-flops are to be buffered by parallel inverters driven by a tree of inverters if necessary such that they can drive 500 fF with reasonable delay.

#### Layout

The bounding box width $W$ and length $L$ for your overall interval timer layout is to obey the following aspect ratio constraints: $1/3 \leq W/L \leq 3$. This keeps your design from being too wide or too high.

To control this aspect ratio, you will need to do the following with **Autofloorplan**:

After you select **Autofloorplan**, you get a form for specifying the **Autofloorplan Options**. The **aspect ratio** is defined as the ratio:

$$\frac{\text{cell’s width } W}{\text{cell’s height } H}$$

You can specify a lower and an upper bound on the aspect ratio. If you specify for example 0.5 and 1.5, the floorplan will have a width that cannot be smaller than half the height and it cannot be larger than double the height.

Note that you cannot be sure that the tool will achieve an exact value of aspect ratio, due to the discrete nature of the cell placement problem.

At the **Autofloorplan Options**, you can also specify the maximum dimensions of the floorplan. If you are shaping the floorplan based on the aspect ratio, the maximum dimensions should be much larger than the actual dimensions of your cell (so that they do not also constrain the floorplanning operation).
You will be performing your layout as a flat standard cell layout. The layout is to be done automatically by using the techniques covered in the second ic station tutorial. After the automatic polycell layout is produced, the VDD and GND interconnects exiting the cell will be too narrow. These are to be manually widened if reasonably possible to at least 10 \( \lambda \). To do this, select the line. From the top menu select:

**Objects -> Change -> Path**

At the menu that will appear at the bottom, select the desired width (e.g. 10 lambda) and select the “end style” to be “normal”. Click on OK.

If you see a message such as:

“Modification of object(s) was not allowed. Net shorts would result.”

you cannot change the width of the line. You can try for a smaller width or if you think that the line cannot be made wider, skip that line.

Note that your grade will depend upon factors including but not limited to the following: 1) correct function, 2) meeting frequency specification, 3) comparative amount of area of your layout to the values of other teams, and 4) comparative worst case power to the values of other teams. If any values are not provided and substantiated as requested, they will be assumed the worst in class. The above factors should be taken into account in your final layout. **Also, note that your layout is to be free of design rule errors.**

**Simulation Environment**

The simulation environment for the counter is as follows:

**Clock Input and Complement:** Directly from voltage sources with \( 0 < t_r \) and \( t_f \leq 0.2 \text{ ns} \).

**Input Signals:** Directly from voltage sources with \( t_r \) and \( t_f \) approximately equal to those of your inverter output.

**Output Loading:** Each of the two outputs from the two flip-flops is have a driver structure described previously loaded with 500 fF; nothing else. There is no added capacitive loading on the rest of the circuit except that extracted by ic or generated during the HSPICE simulation.

**Functional Simulation**

Find a series of input combinations and clock input values that will extensively test your comparator. Since the simulation will be fairly time-consuming, try to use as few patterns as possible that will test most of the paths through your design.

**Speed Simulation**

Again, simulation is likely to be time-consuming. So you are to do a few clock cycles or so with those combinations and a signal change if needed that cause signals to propagate along the longest paths in your circuit, the critical paths with combinational part of length \( N_{crit} \). Do not just do the above blindly; make sure they are worst case paths.
You are to determine that your circuit will operate at 120 MHz with inputs set to propagate signals along the critical paths. In addition, by varying the clock frequency or measuring critical path delays, you are to estimate the maximum clock frequency at which your circuit will operate.

In summary, from these simulations, you are to extract two answers: 1) Can your comparator run at 120 MHz? and 2) What is the estimated maximum frequency at which your comparator can operate?

**Power Simulation**

Estimate the average power dissipation of your circuit by finding the average power for at least five of what you believe to be worst case input changes on the comparator, i.e., five sequences of two input combinations each applied at 120 MHz that will cause the maximum number of gate output changes. For this simulation, the input flip-flops should be removed from the HSPICE simulation model so that all inputs change simultaneously.

**Final Report**

Your final report is to include the following material. You will be penalized for any missing items.

**Comparator Characterization**

Complete the table on the next page and the associated text to partially characterize your comparator.

**Layouts**

Submit each unique cell layout, e.g., inverter, NAND with 2-inputs, NAND with 4 inputs, flip-flop, and complete layout. These should be such that they are not an unintelligible mess, i.e., should show only the current level of the layout hierarchy. The layouts should be labeled as needed to permit easy visualization. Use the color postscript file method for printing (to avoid the “black layout” problem), but not the color printer unless you are wealthy!

**Simulation Outputs**

Give final plots from simulations specified or alternative simulations that are appropriate for your design. Briefly and clearly explain each simulation experiment; annotate the simulation outputs as needed to show applied inputs and the correctness of the outputs and the measurement of the clock periods or delay times.

**Team Contributions**

Summarize the contributions of each team member to each of the four project phases. In a table, include design, layout, and simulation for each phase for a total of 11 tasks (no layout for the first phase) and give in two columns, the percentage contribution of each team member in performing the task. If there are other tasks that you believe were important, add them at the end of the table.
Final Comparator Characterization:

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Does your comparator, based on simulation measurements, run with a clock of <strong>110 MHz</strong>?</td>
<td>Circle one: Yes No Explain as item 1 on a separate sheet how you arrived at your answer for this and the following question.</td>
</tr>
<tr>
<td>What is the estimated maximum frequency of operation of your comparator based on simulation measurements?</td>
<td></td>
</tr>
<tr>
<td><strong>W</strong> for complete layout in mm</td>
<td></td>
</tr>
<tr>
<td><strong>L</strong> for complete layout in mm</td>
<td></td>
</tr>
<tr>
<td><strong>Bounding box area</strong> for complete layout in mm²</td>
<td></td>
</tr>
<tr>
<td><strong>Pavg</strong> for comparator simulation in mW</td>
<td></td>
</tr>
<tr>
<td>Smallest value of <strong>V_{th}</strong> anywhere in the circuit</td>
<td></td>
</tr>
<tr>
<td>Largest value of <strong>V_{th}</strong> anywhere in the circuit</td>
<td></td>
</tr>
<tr>
<td>Lowest value of <strong>NM_{L}</strong> anywhere in the circuit</td>
<td></td>
</tr>
<tr>
<td>Lowest value of <strong>NM_{H}</strong> anywhere in the circuit</td>
<td></td>
</tr>
</tbody>
</table>